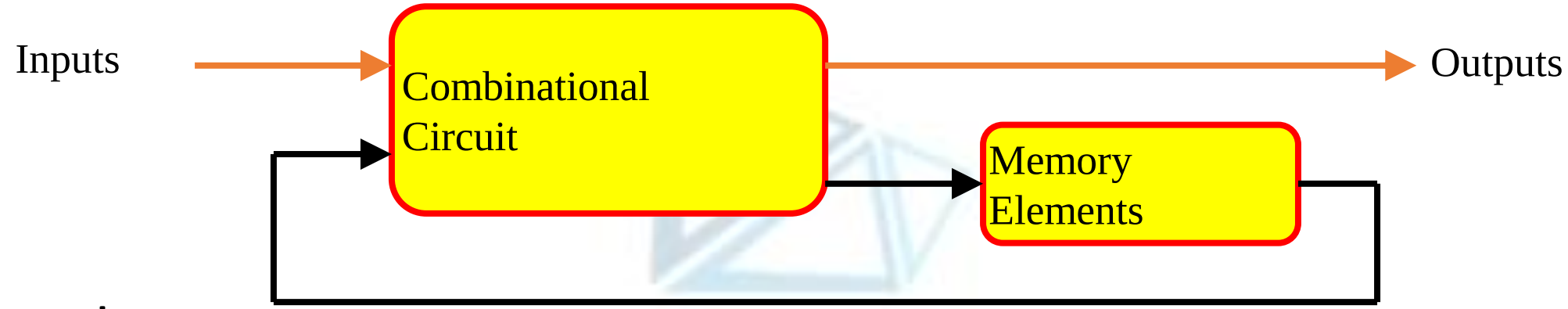
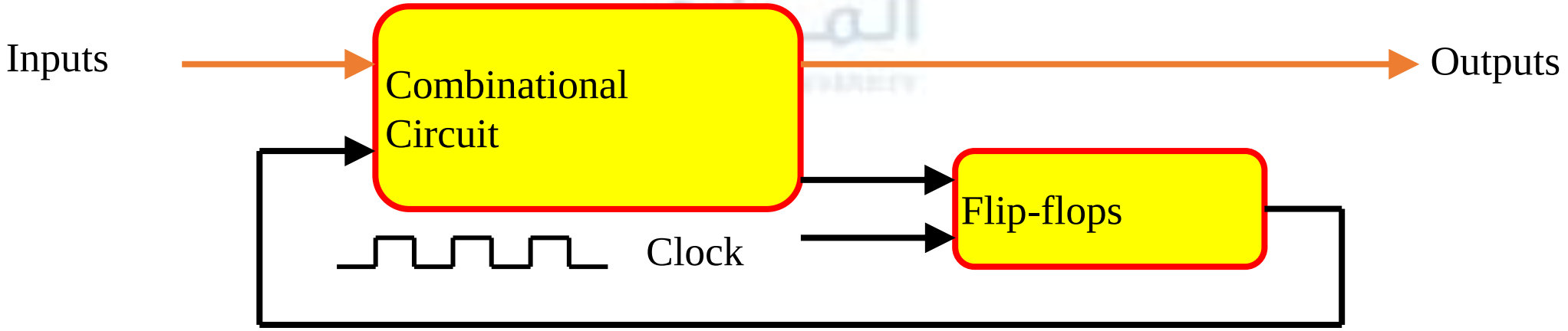
# Sequential Circuits

- Asynchronous

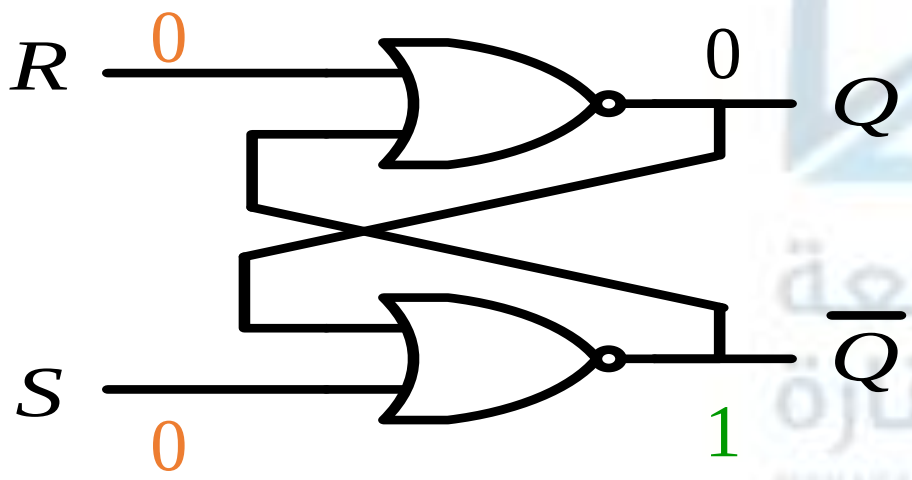



- Synchronous



# Latches

- *SR* Latch



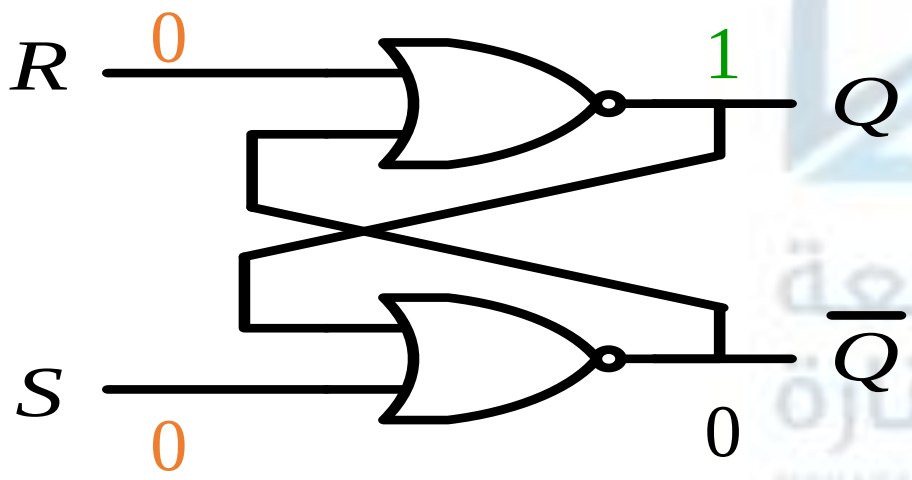

| $S$ $R$ $Q_0$ | $Q$ | $Q'$ |
|---|---|---|
| 0 0 0 | 0 | 1 |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |

$Q = Q_0$

Initial Value

# Latches

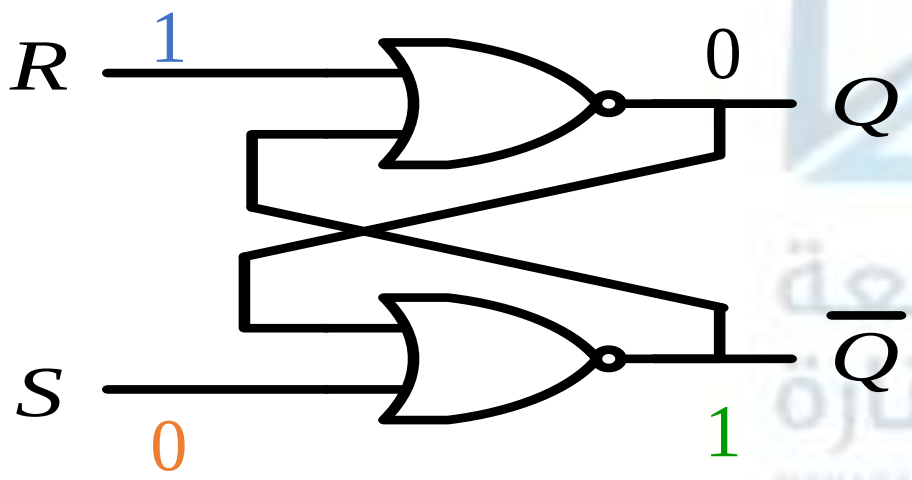
- *SR* Latch




| $S$ $R$ $Q_0$ | $Q$ | $Q'$ | |
|---|---|---|---|
| 0 0 0 | 0 | 1 | $Q = Q_0$ |
| 0 0 1 | 1 | 0 | $Q = Q_0$ |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

# Latches

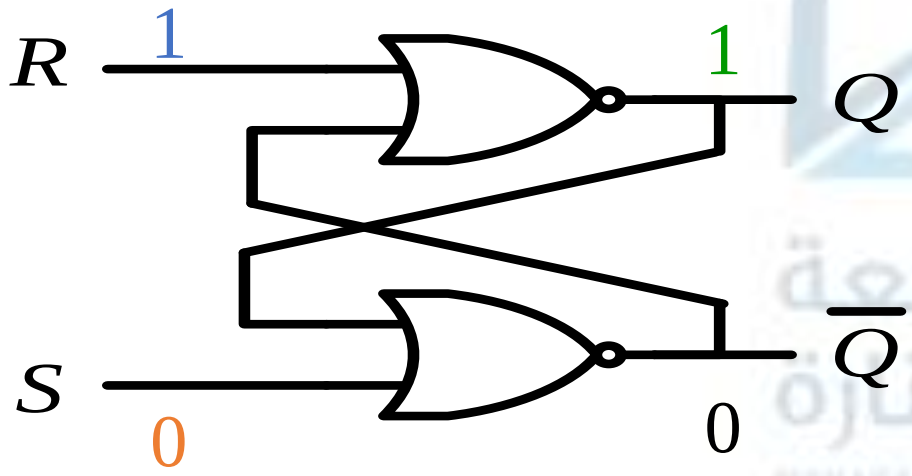
- *SR* Latch




| $S$ $R$ $Q_0$ | $Q$ | $Q'$ | |
|---|---|---|---|
| 0 0 0 | 0 | 1 | $Q = Q_0$ |
| 0 0 1 | 1 | 0 | |
| 0 1 0 | 0 | 1 | $Q = 0$ |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

# Latches

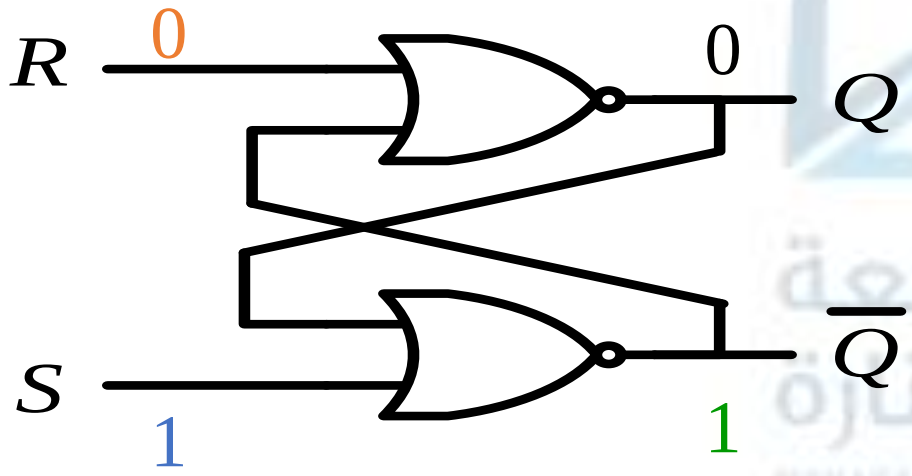
- *SR* Latch




| S | R | $Q_0$ | Q | Q' | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | $Q = Q_0$ |
| 0 | 0 | 1 | 1 | 0 | |
| 0 | 1 | 0 | 0 | 1 | $Q = 0$ |
| 0 | 1 | 1 | 0 | 1 | $Q = 0$ |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

# Latches

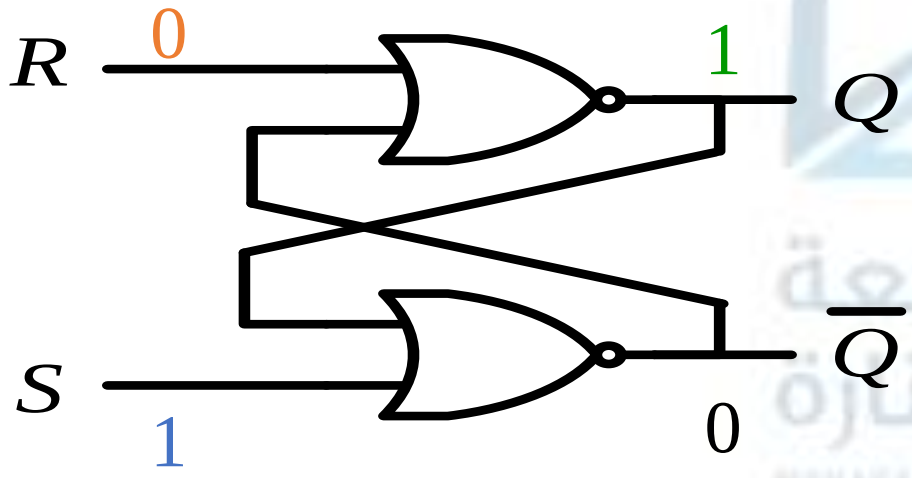
- *SR* Latch




| S R $Q_0$ | Q | Q' | |
|---|---|---|---|
| 0 0 0 | 0 | 1 | $Q = Q_0$ |
| 0 0 1 | 1 | 0 | |
| 0 1 0 | 0 | 1 | $Q = 0$ |
| 0 1 1 | 0 | 1 | |
| 1 0 0 | 1 | 0 | $Q = 1$ |
| | | | |
| | | | |
| | | | |

# Latches

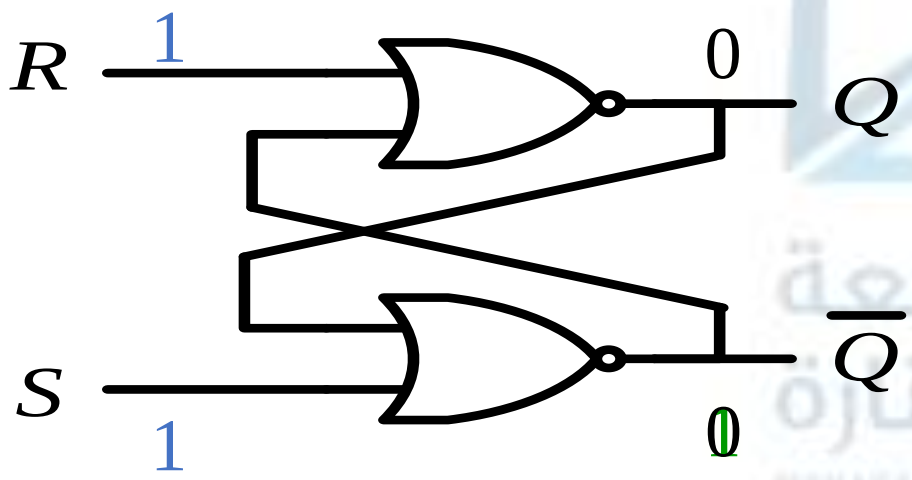
- *SR* Latch




| S | R | $Q_0$ | Q | Q' | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | $Q = Q_0$ |
| 0 | 0 | 1 | 1 | 0 | |
| 0 | 1 | 0 | 0 | 1 | $Q = 0$ |
| 0 | 1 | 1 | 0 | 1 | |
| 1 | 0 | 0 | 1 | 0 | $Q = 1$ |
| 1 | 0 | 1 | 1 | 0 | $Q = 1$ |
| | | | | | |
| | | | | | |

# Latches

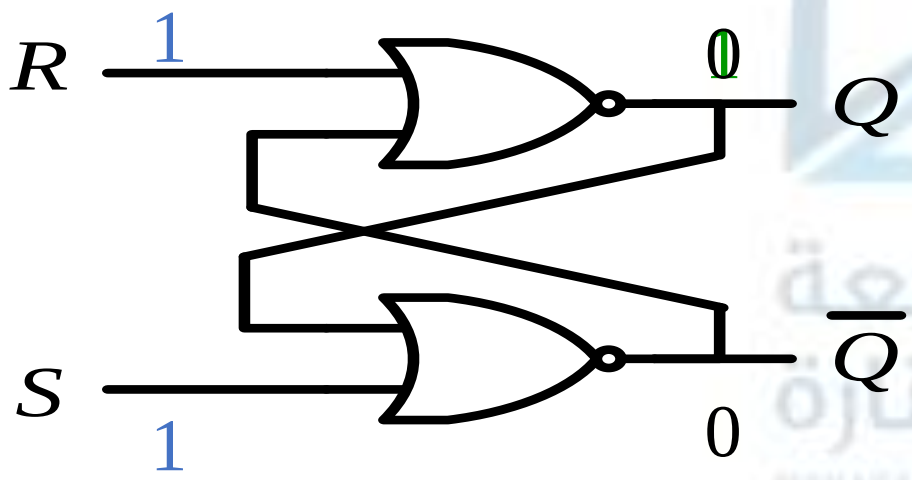
- *SR* Latch




| S | R | $Q_0$ | Q | Q' | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | $Q = Q_0$ |
| 0 | 0 | 1 | 1 | 0 | |
| 0 | 1 | 0 | 0 | 1 | $Q = 0$ |
| 0 | 1 | 1 | 0 | 1 | |
| 1 | 0 | 0 | 1 | 0 | $Q = 1$ |
| 1 | 0 | 1 | 1 | 0 | |
| 1 | 1 | 0 | 0 | 0 | $Q = Q'$ |
| | | | | | |

# Latches

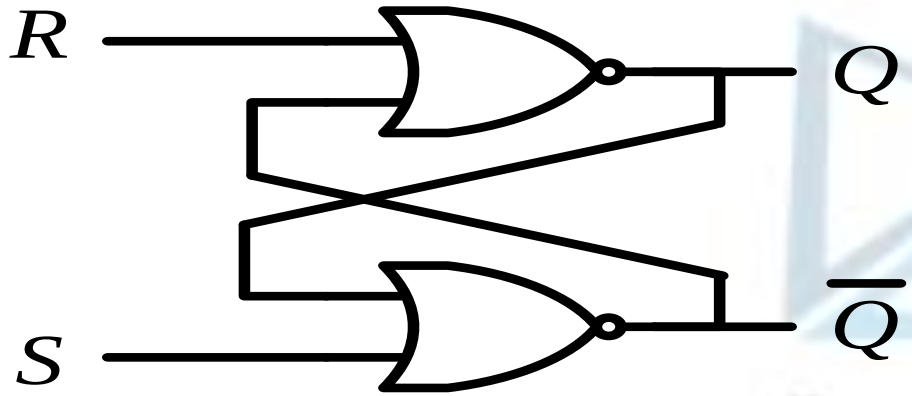
- *SR* Latch



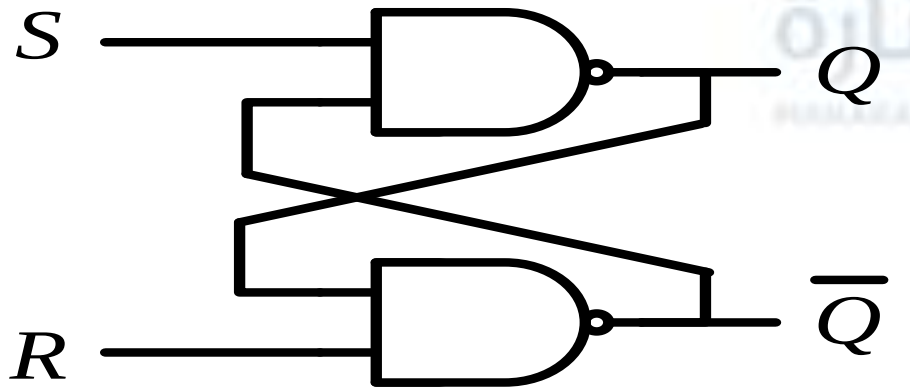

| S | R | $Q_0$ | Q | Q' | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | $Q = Q_0$ |
| 0 | 0 | 1 | 1 | 0 | |
| 0 | 1 | 0 | 0 | 1 | $Q = 0$ |
| 0 | 1 | 1 | 0 | 1 | |
| 1 | 0 | 0 | 1 | 0 | $Q = 1$ |
| 1 | 0 | 1 | 1 | 0 | |
| 1 | 1 | 0 | 0 | 0 | $Q = Q'$ |
| 1 | 1 | 1 | 0 | 0 | $Q = Q'$ |

# Latches

- *SR* Latch



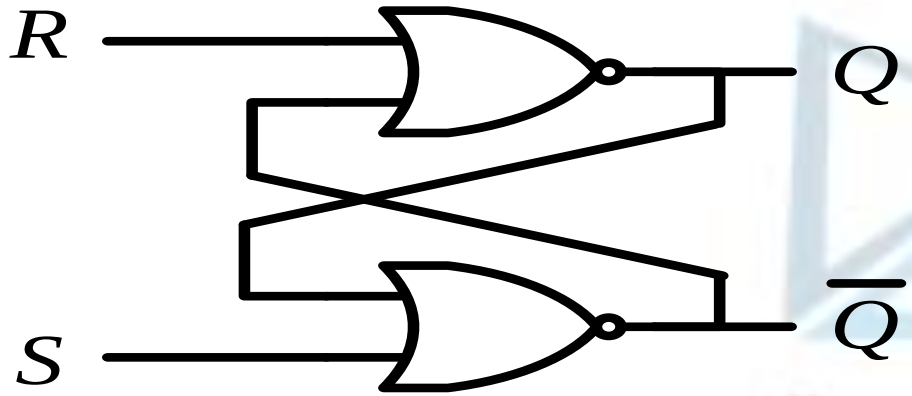

| S R | Q | |
|---|---|---|
| 0 0 | $Q_0$ | No change |
| 0 1 | 0 | Reset |
| 1 0 | 1 | Set |
| 1 1 | $Q=Q'=0$ | Invalid |



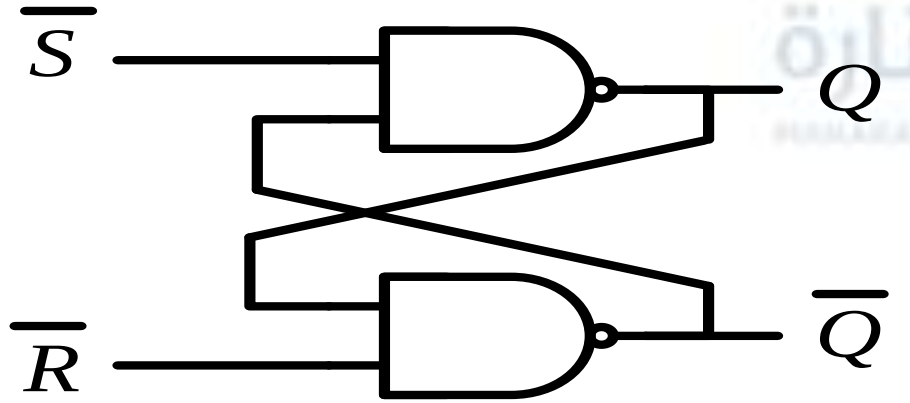

| S R | Q | |
|---|---|---|
| 0 0 | $Q=Q'=1$ | Invalid |
| 0 1 | 1 | Set |
| 1 0 | 0 | Reset |
| 1 1 | $Q_0$ | No change |

# Latches

- *SR* Latch



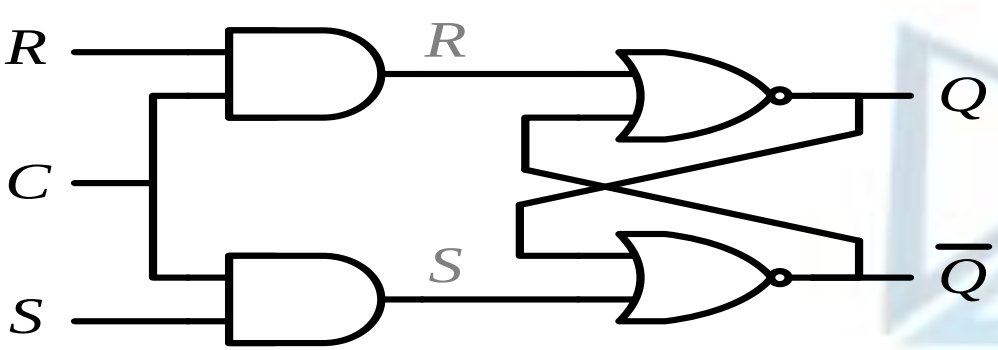

| S R | Q | |
|---|---|---|
| 0 0 | $Q_0$ | No change |
| 0 1 | 0 | Reset |
| 1 0 | 1 | Set |
| 1 1 | $Q=Q'=0$ | Invalid |

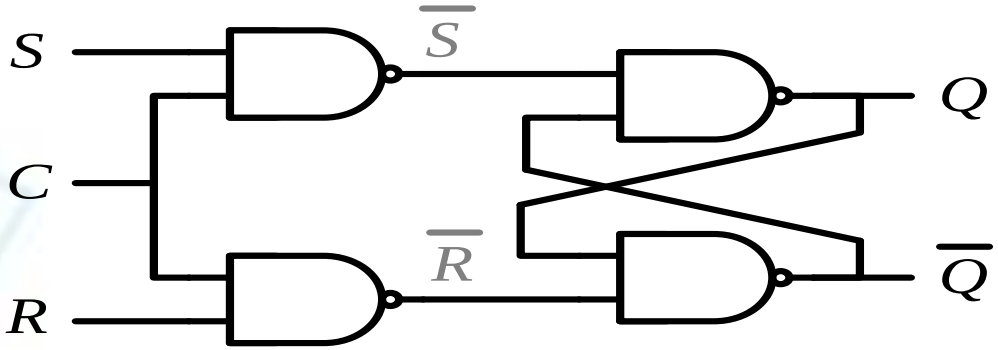



| S' R' | Q | |
|---|---|---|
| 0 0 | $Q=Q'=1$ | Invalid |
| 0 1 | 1 | Set |
| 1 0 | 0 | Reset |
| 1 1 | $Q_0$ | No change |

# Controlled Latches

- *SR* Latch with Control Input

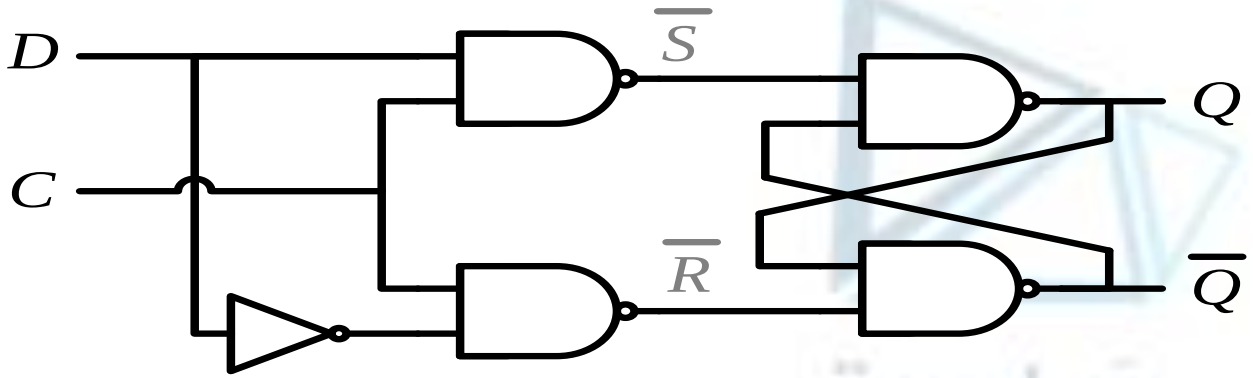



| C S R | Q | |
|---|---|---|
| 0 x x | $Q_0$ | No change |
| 1 0 0 | $Q_0$ | No change |
| 1 0 1 | 0 | Reset |
| 1 1 0 | 1 | Set |
| 1 1 1 | $Q=Q'$ | Invalid |

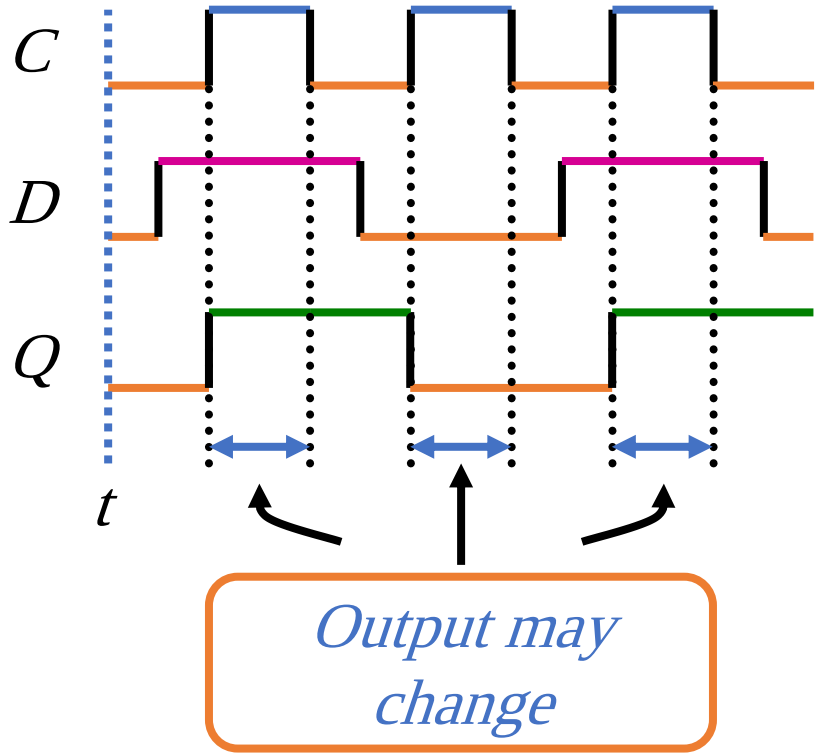
# Controlled Latches

- *D* Latch (*D* = *Data*)



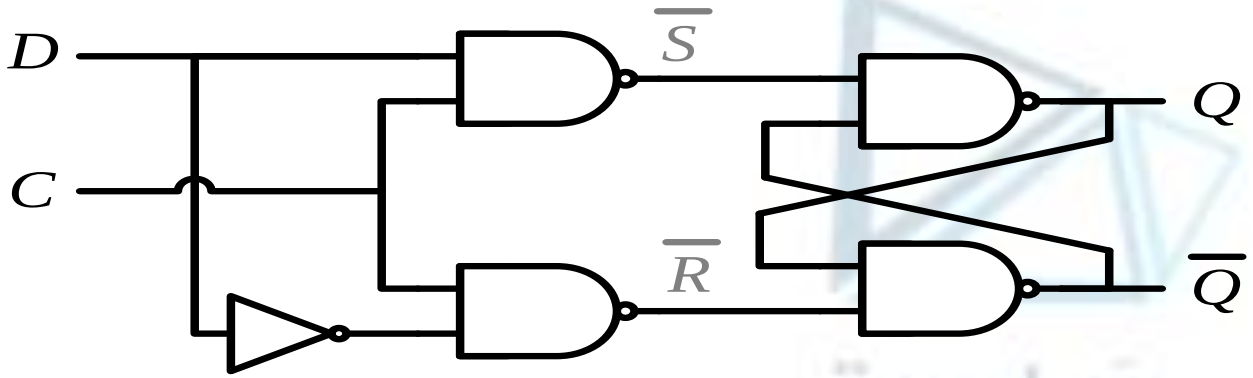

| C | D | Q | |
|---|---|---|---|
| 0 | x | $Q_0$ | No change |
| 1 | 0 | 0 | Reset |
| 1 | 1 | 1 | Set |

*Timing Diagram*



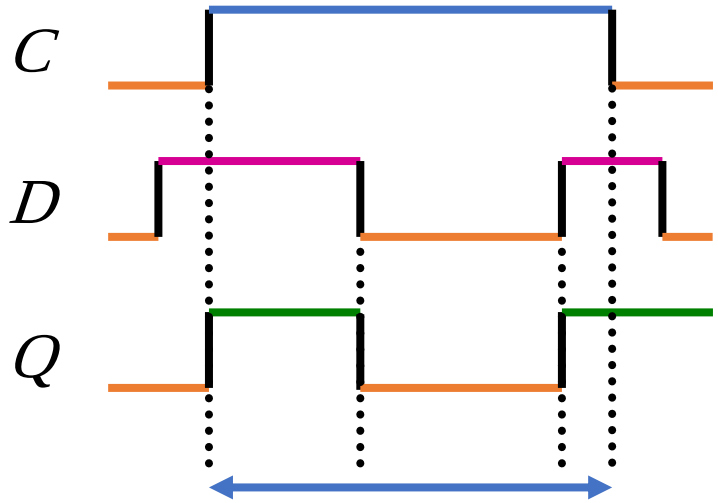
# Controlled Latches

- *D* Latch (*D* = *Data*)



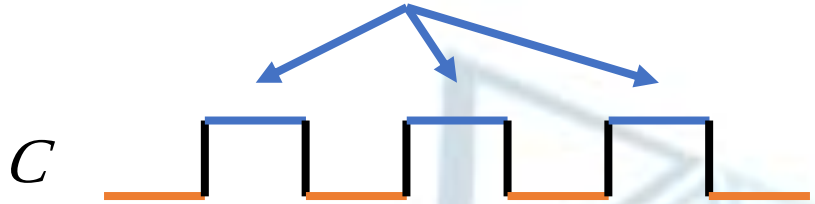

| C | D | Q | |
|---|---|---|---|
| 0 | x | $Q_0$ | No change |
| 1 | 0 | 0 | Reset |
| 1 | 1 | 1 | Set |

*Timing Diagram*

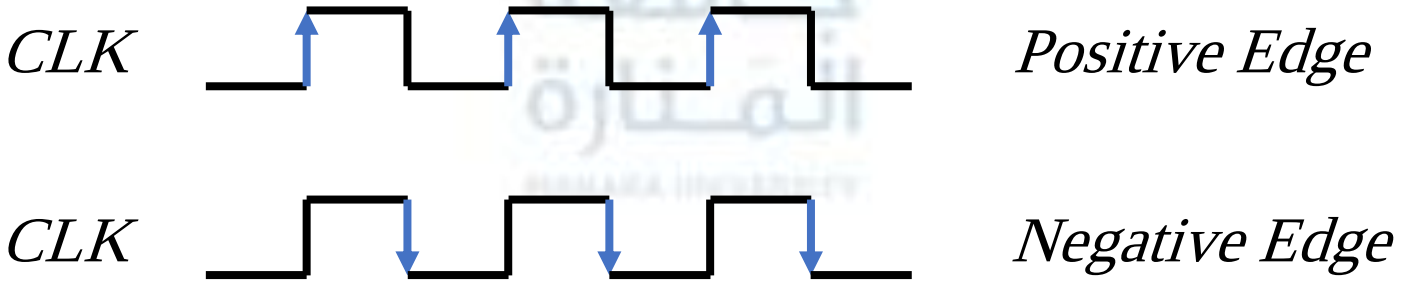


# Flip-Flops

- Controlled latches are level-triggered

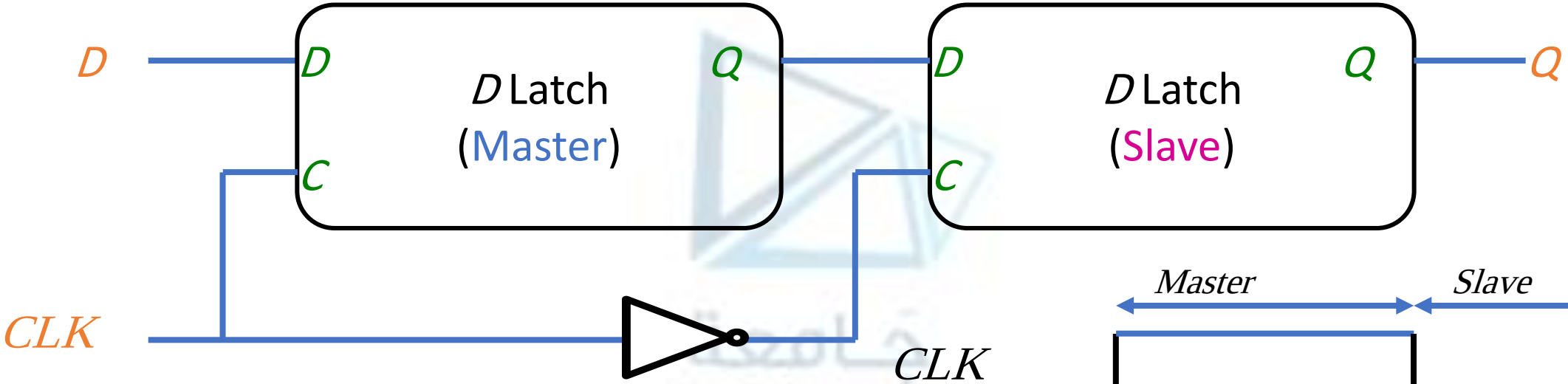


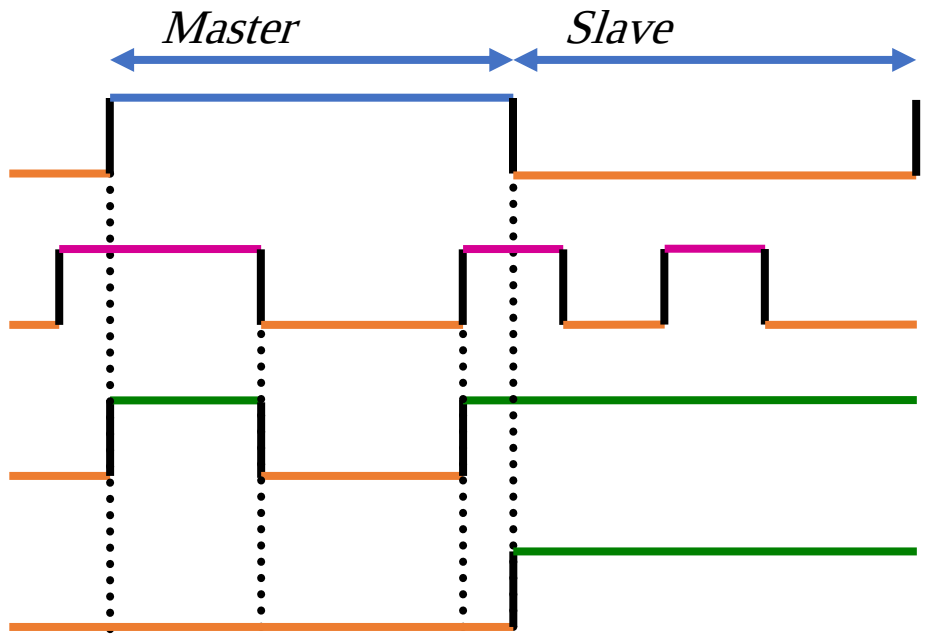

- Flip-Flops are edge-triggered



# Flip-Flops

- Master-Slave *D* Flip-Flop

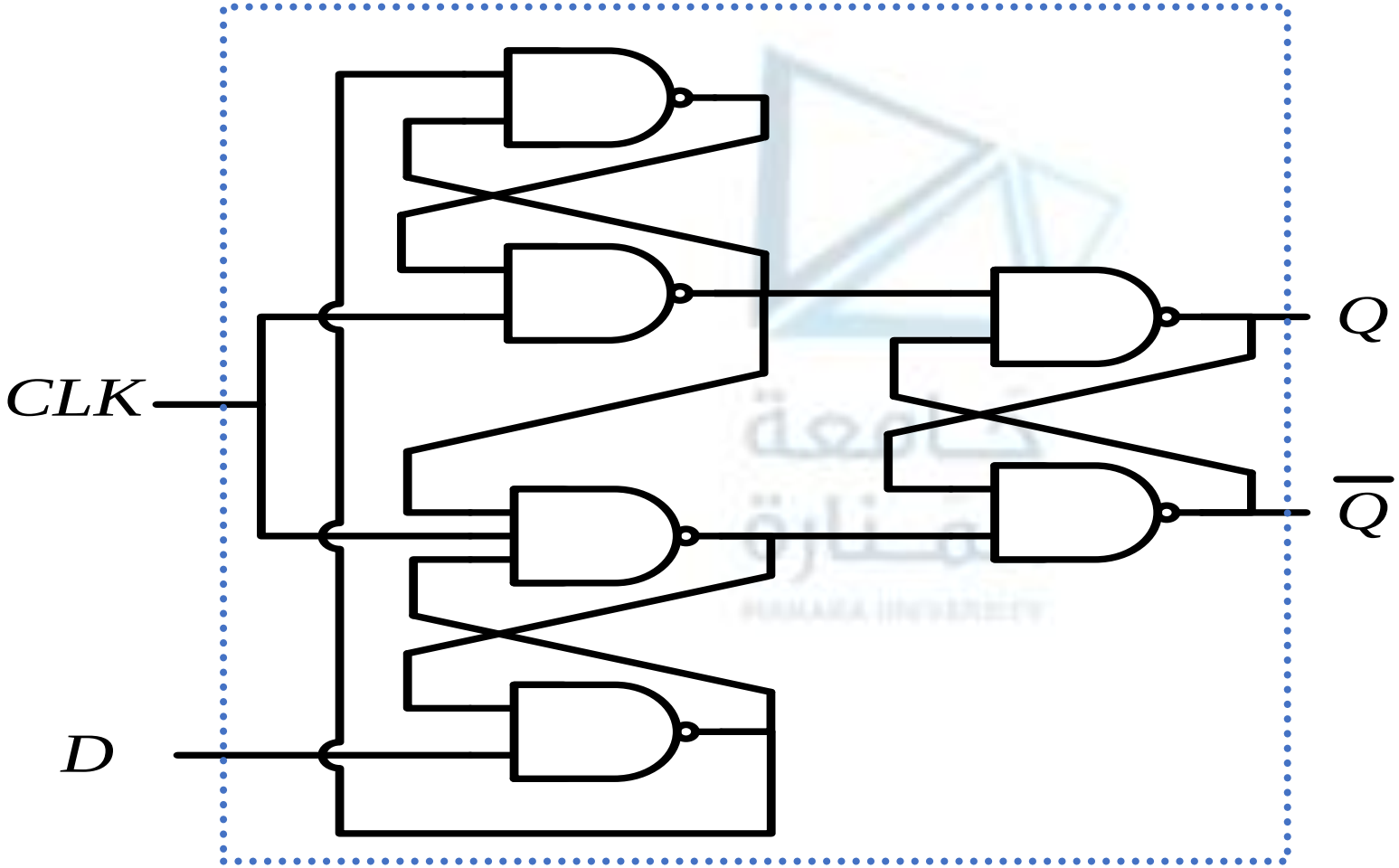


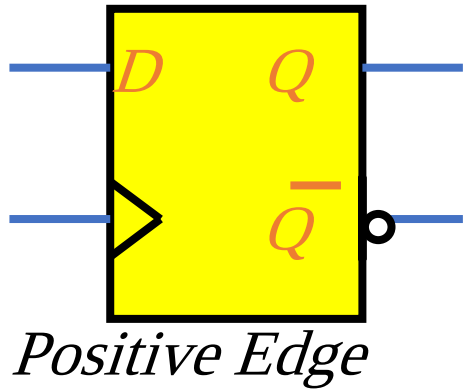




Looks like it is negative edge-triggered

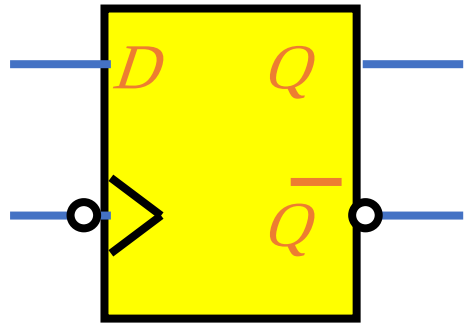
# Flip-Flops

- Edge-Triggered *D* Flip-Flop



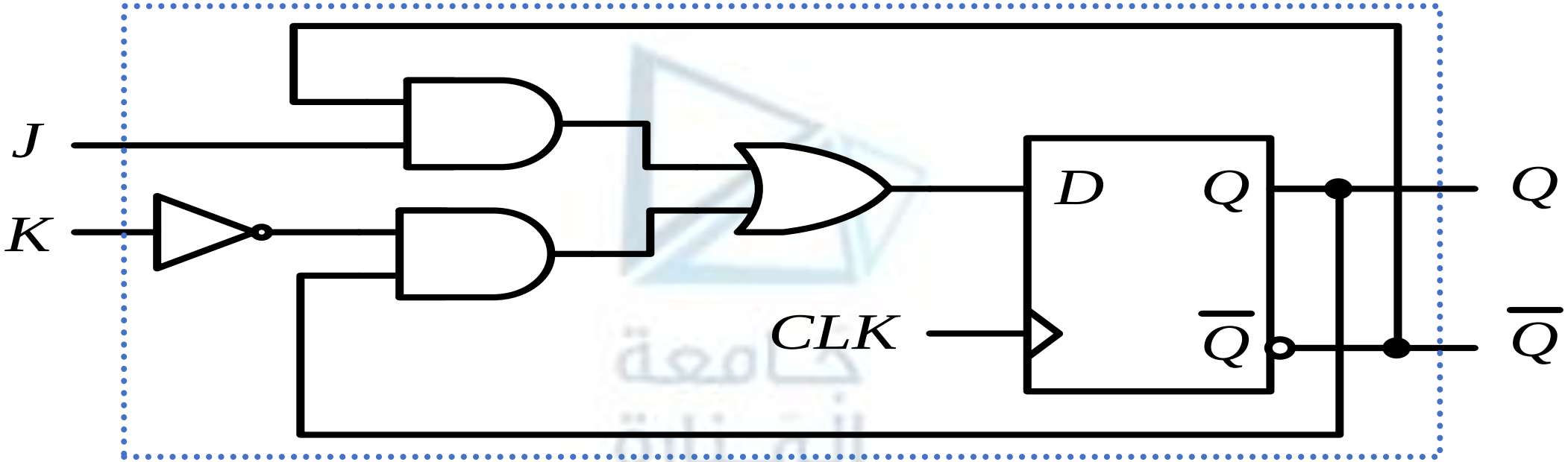

*Positive Edge*



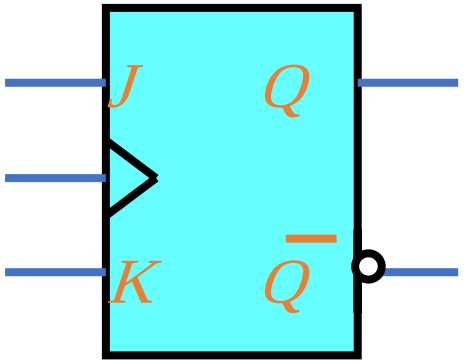

*Negative Edge*

# Flip-Flops

- *JK* Flip-Flop

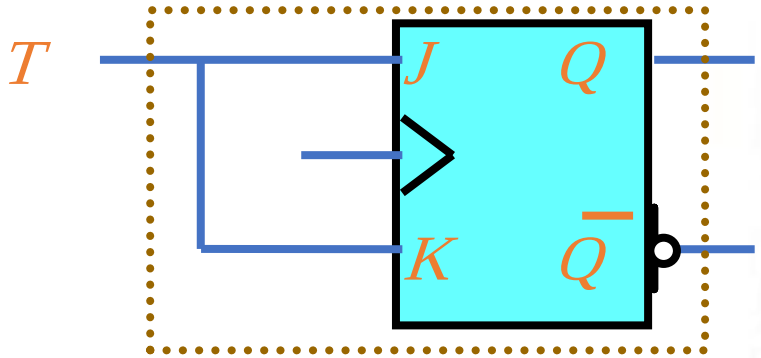


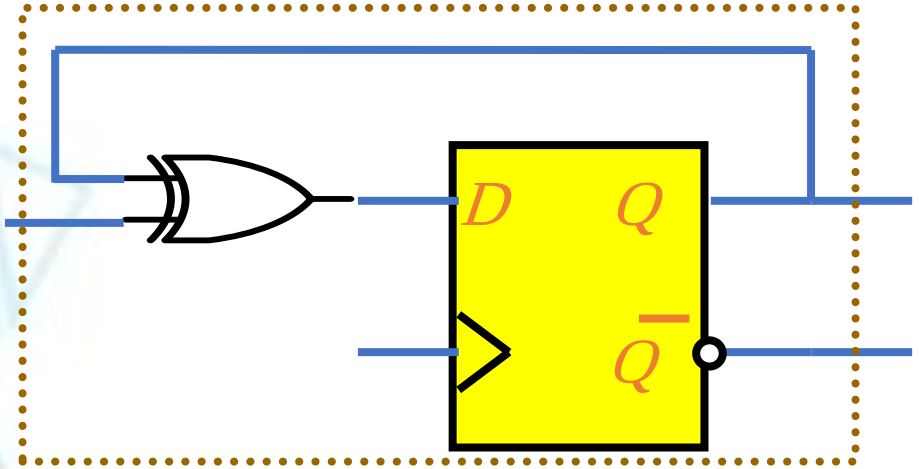

$$D = JQ' + K'Q$$



# Flip-Flops

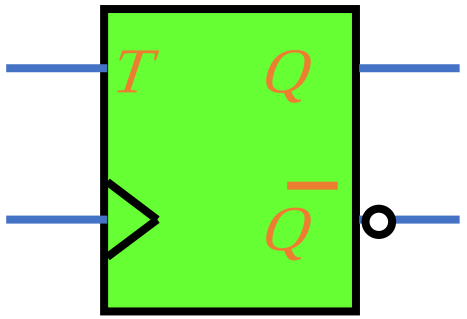
- *T* Flip-Flop



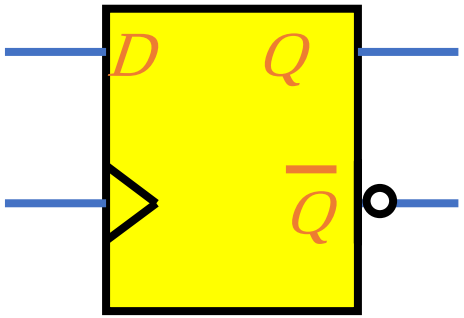




$$D = JQ' + K'Q$$

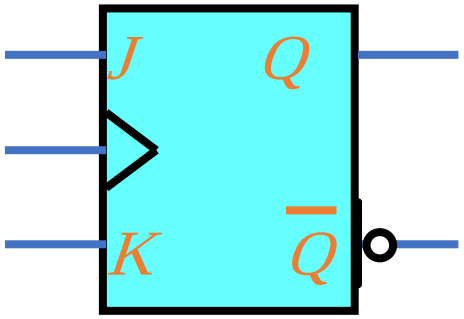
$$D = TQ' + T'Q = T \oplus Q$$



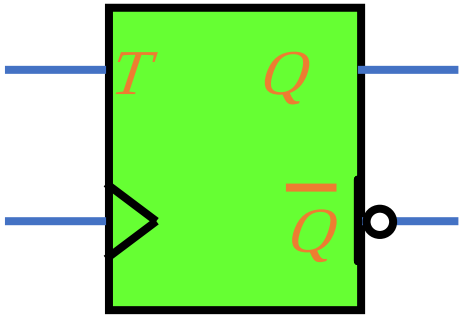
# Flip-Flop Characteristic Tables




| D | Q(t+1) | |
|---|---|---|
| 0 | 0 | Reset |
| 1 | 1 | Set |

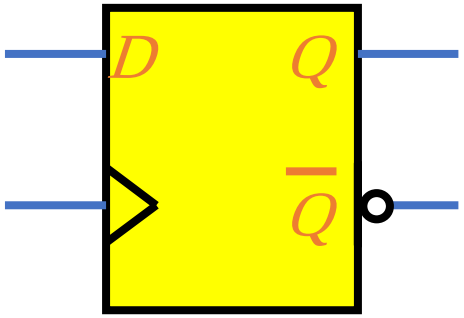



| J | K | Q(t+1) | |
|---|---|---|---|
| 0 | 0 | Q(t) | No change |
| 0 | 1 | 0 | Reset |
| 1 | 0 | 1 | Set |
| 1 | 1 | Q'(t) | Toggle |



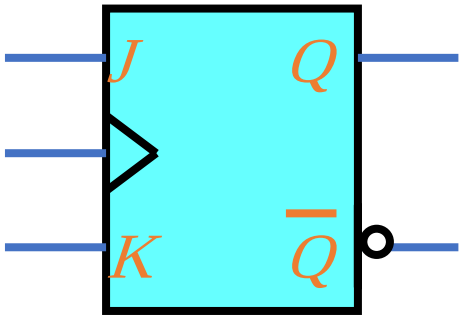

| T | Q(t+1) | |
|---|---|---|
| 0 | Q(t) | No change |
| 1 | Q'(t) | Toggle |

# Flip-Flop Characteristic Equations



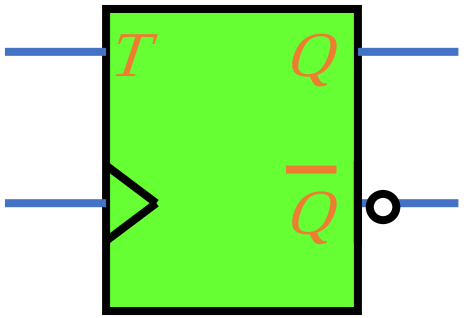

| D | Q(t+1) |
|---|---|
| 0 | 0 |
| 1 | 1 |

$$Q(t+1) = D$$




| J | K | Q(t+1) |
|---|---|---|
| 0 | 0 | Q(t) |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | Q'(t) |

$$Q(t+1) = JQ' + K'Q$$

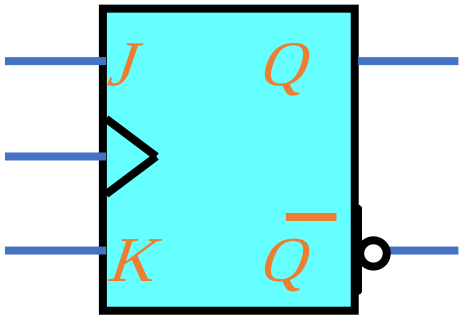



| T | Q(t+1) |
|---|---|
| 0 | Q(t) |
| 1 | Q'(t) |

$$Q(t+1) = T \oplus Q$$

# Flip-Flop Characteristic Equations

- Analysis / Derivation

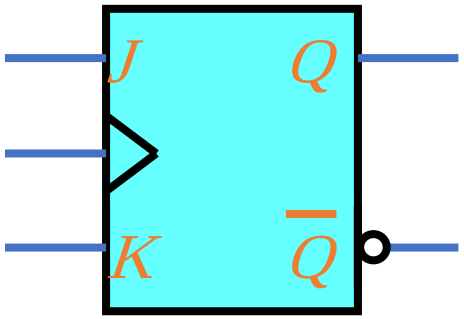



| J | K | Q(t) | Q(t+1) |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |

No change

# Flip-Flop Characteristic Equations

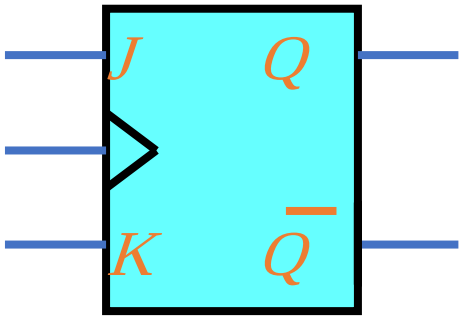
- Analysis / Derivation




| $J$ | $K$ | $Q(t)$ | $Q(t+1)$ | |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | No change |
| 0 | 0 | 1 | 1 | |
| 0 | 1 | 0 | 0 | Reset |
| 0 | 1 | 1 | 0 | |
| 1 | 0 | 0 | | |
| 1 | 0 | 1 | | |
| 1 | 1 | 0 | | |
| 1 | 1 | 1 | | |

# Flip-Flop Characteristic Equations

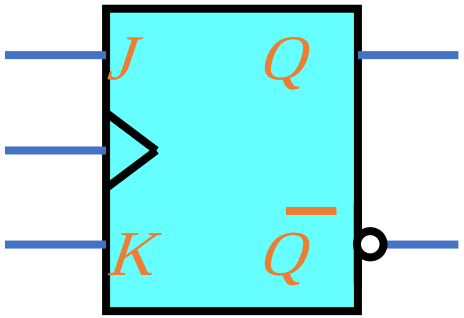
- Analysis / Derivation




| $J$ | $K$ | $Q(t)$ | $Q(t+1)$ | |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | No change |
| 0 | 0 | 1 | 1 | |
| 0 | 1 | 0 | 0 | Reset |
| 0 | 1 | 1 | 0 | |
| 1 | 0 | 0 | 1 | Set |
| 1 | 0 | 1 | 1 | |
| 1 | 1 | 0 | | |
| 1 | 1 | 1 | | |

# Flip-Flop Characteristic Equations

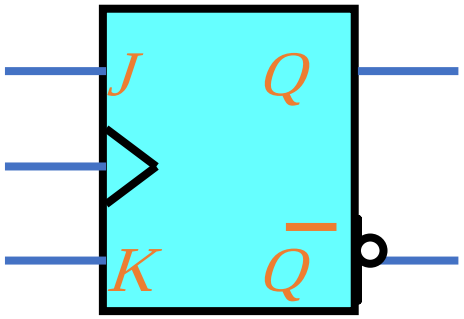
- Analysis / Derivation



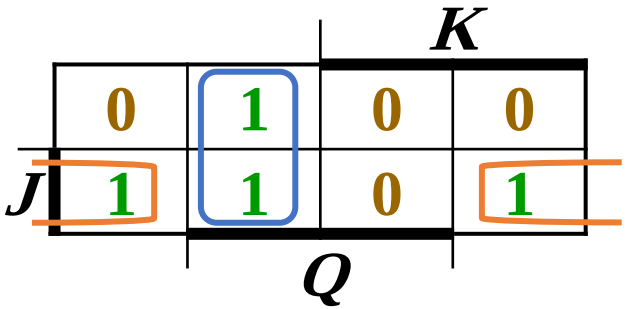

| $J$ | $K$ | $Q(t)$ | $Q(t+1)$ | |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | No change |
| 0 | 0 | 1 | 1 | |
| 0 | 1 | 0 | 0 | Reset |
| 0 | 1 | 1 | 0 | |
| 1 | 0 | 0 | 1 | Set |
| 1 | 0 | 1 | 1 | |
| 1 | 1 | 0 | 1 | Toggle |
| 1 | 1 | 1 | 0 | |

# Flip-Flop Characteristic Equations

- Analysis / Derivation



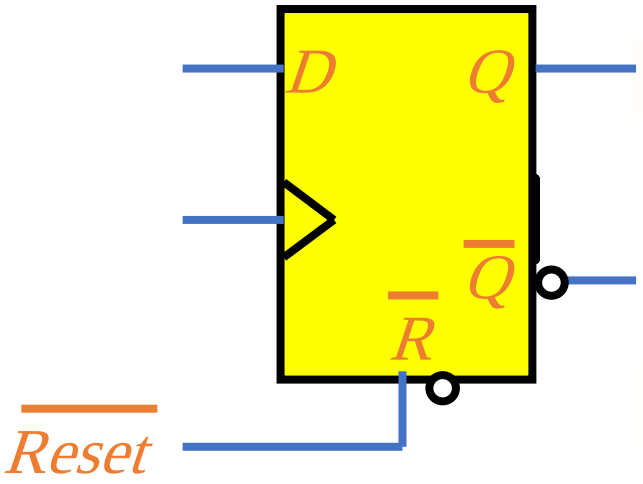

| J | K | Q(t) | Q(t+1) |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |




$$Q(t+1) = JQ' + K'Q$$

# Flip-Flops with Direct Inputs

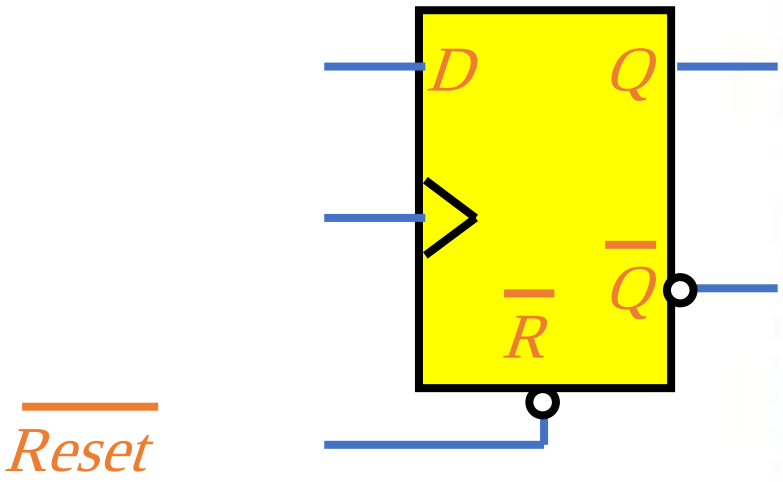
- Asynchronous Reset




| $R'$ | $D$ | $CLK$ | $Q(t+1)$ |
|---|---|---|---|
| 0 | x | x | 0 |
| | | | |
| | | | |

# Flip-Flops with Direct Inputs

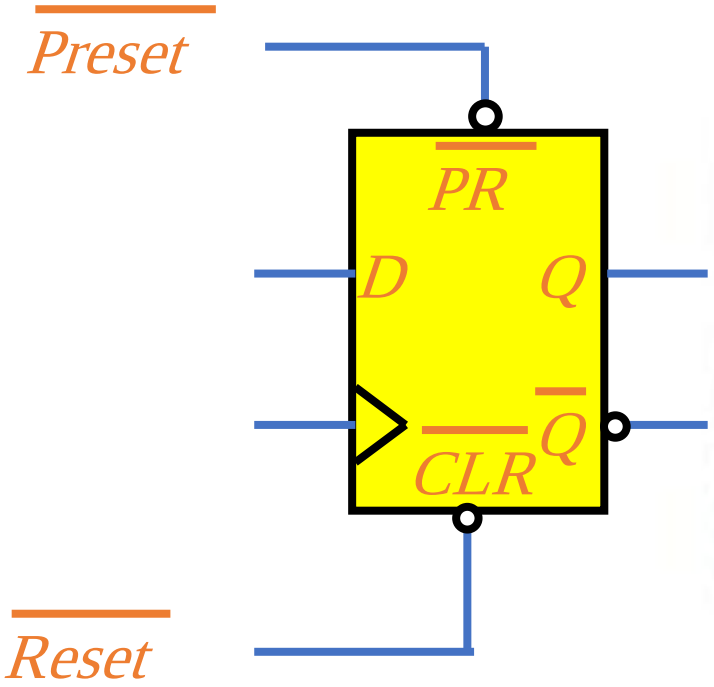
- Asynchronous Reset




| $R'$ | $D$ | $CLK$ | $Q(t+1)$ |
|---|---|---|---|
| 0 | x | x | 0 |
| 1 | 0 | ↑ | 0 |
| 1 | 1 | ↑ | 1 |

# Flip-Flops with Direct Inputs

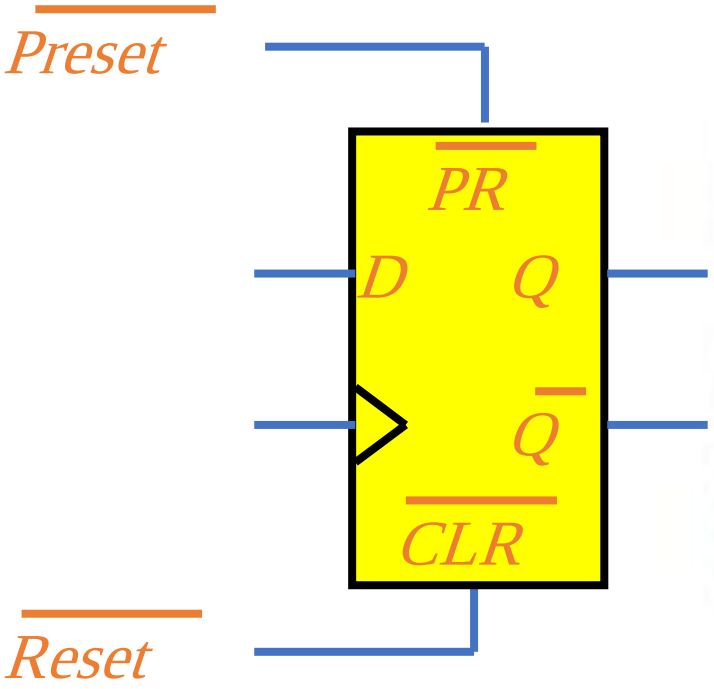
- Asynchronous Preset and Clear




| PR' | CLR' | D | CLK | Q(t+1) |
|---|---|---|---|---|
| 1 | 0 | x | x | 0 |
| | | | | |
| | | | | |
| | | | | |

# Flip-Flops with Direct Inputs

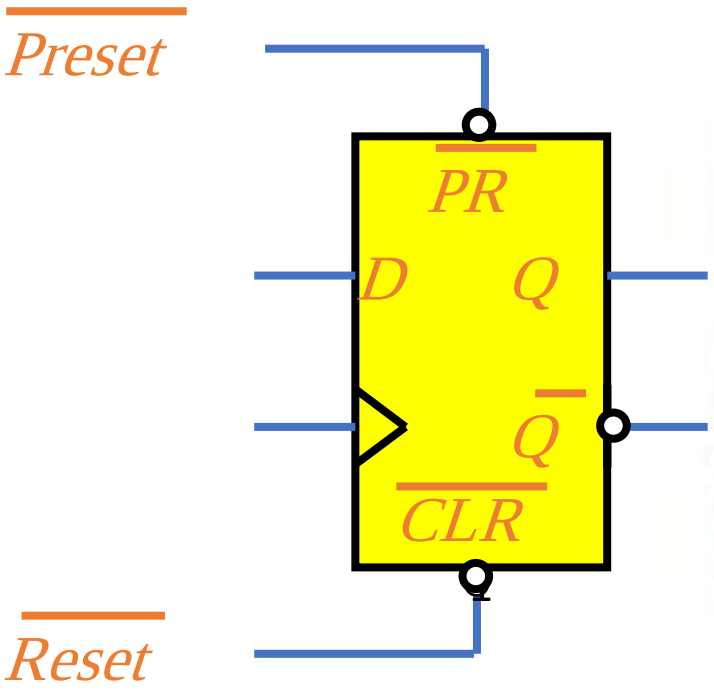
- Asynchronous Preset and Clear




| PR' | CLR' | D | CLK | Q(t+1) |
|---|---|---|---|---|
| 1 | 0 | x | x | 0 |
| 0 | 1 | x | x | 1 |
| | | | | |
| | | | | |

# Flip-Flops with Direct Inputs

- Asynchronous Preset and Clear



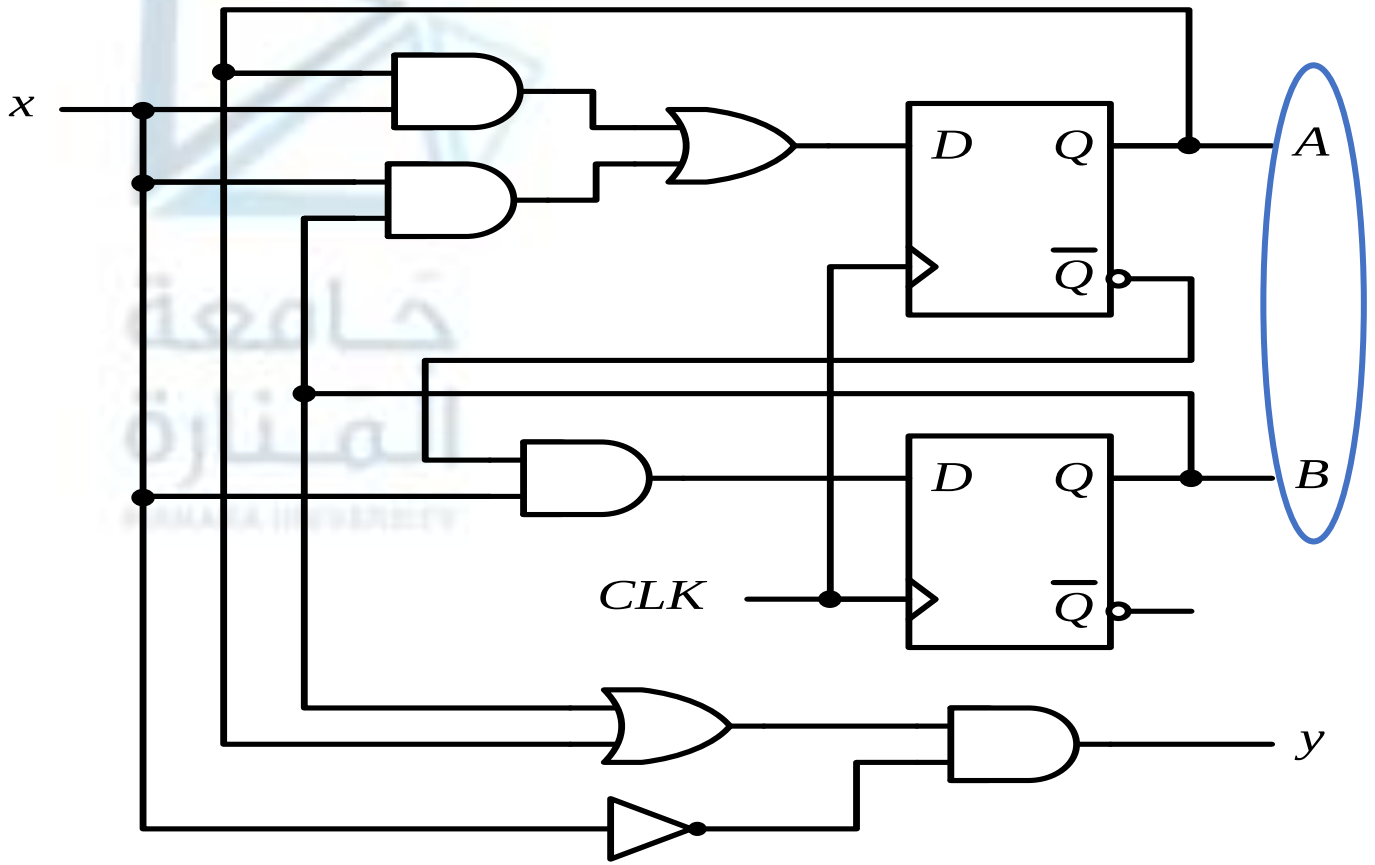

| PR' | CLR' | D | CLK | Q(t+1) |
|---|---|---|---|---|
| 1 | 0 | x | x | 0 |
| 0 | 1 | x | x | 1 |
| 1 | 1 | 0 | ↑ | 0 |
| 1 | 1 | 1 | ↑ | 1 |

# Analysis of Clocked Sequential Circuits

- The State
  - State = Values of all Flip-Flops

Example

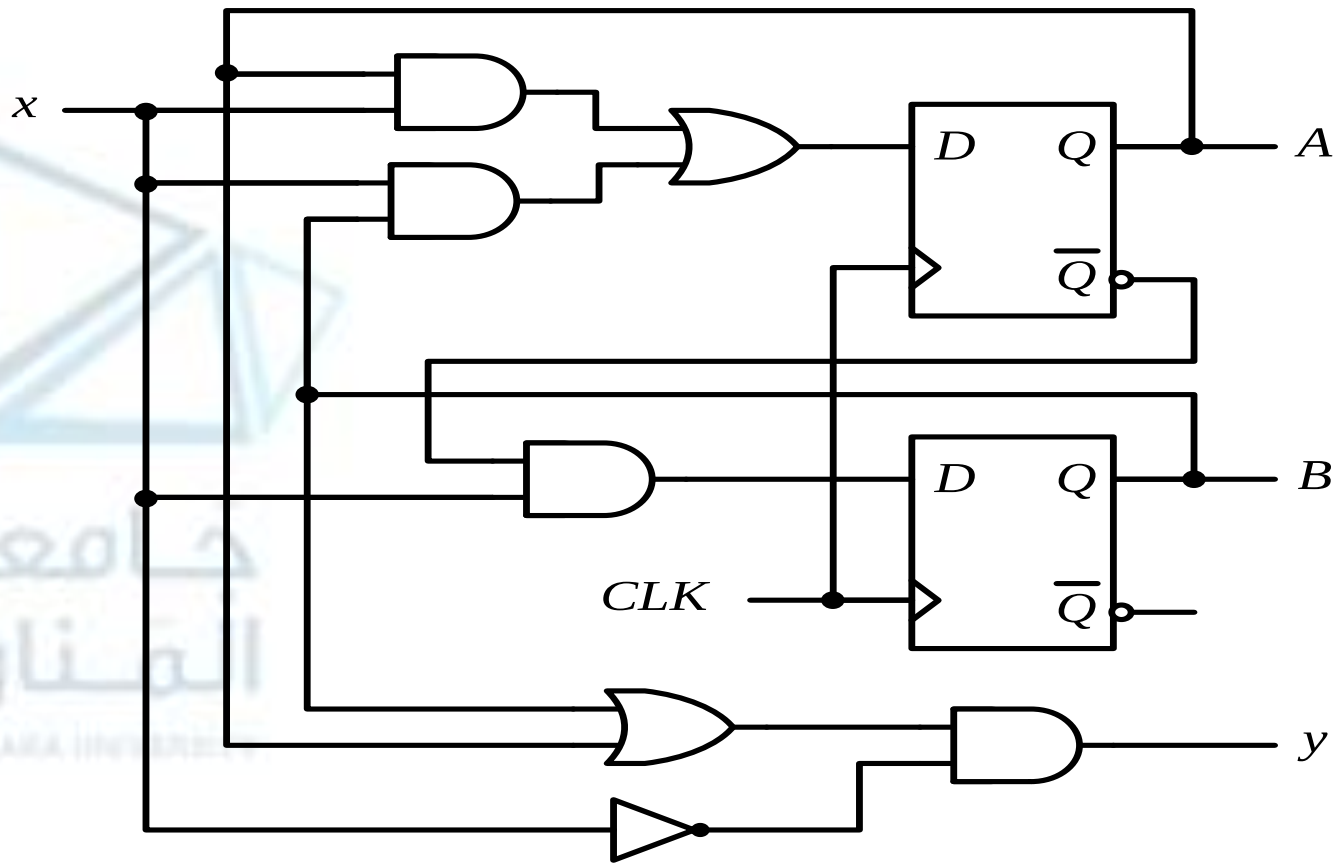
$A\ B = 0\ 0$



# Analysis of Clocked Sequential Circuits

- State Equations

$$A(t+1) = D_A$$
$$= A(t)\,x(t) + B(t)\,x(t)$$
$$= A\,x + B\,x$$
$$B(t+1) = D_B$$
$$= A'(t)\,x(t)$$
$$= A'\,x$$
$$y(t) = [A(t) + B(t)]\,x'(t)$$
$$= (A + B)\,x'$$

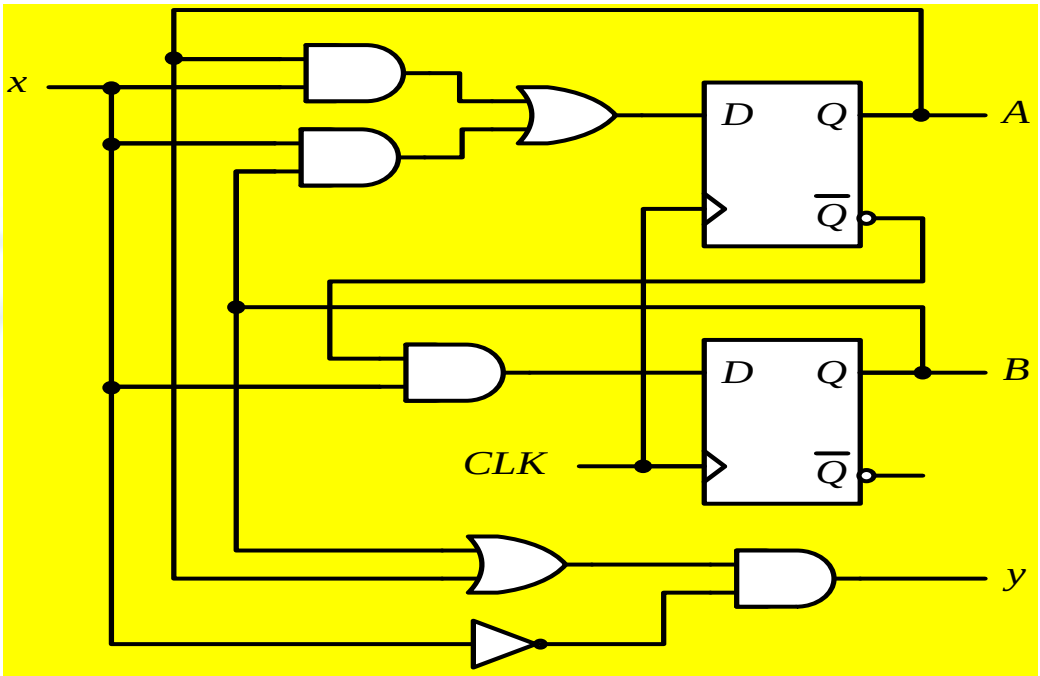


# Analysis of Clocked Sequential Circuits

- State Table (Transition Table)

| Present State | | Input | Next State | | Output |
|---|---|---|---|---|---|
| *A* | *B* | *x* | *A* | *B* | *y* |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 |

$t$ $t+1$ $t$



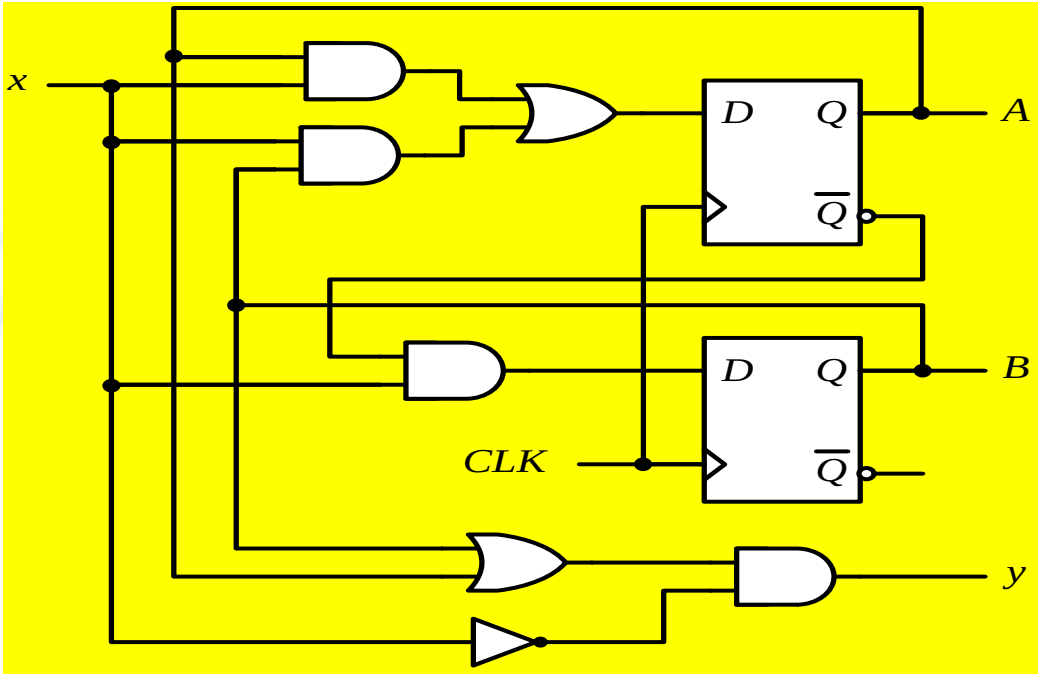

$$A(t+1) = A\,x + B\,x$$
$$B(t+1) = A'\,x$$
$$y(t) = (A + B)\,x'$$

# Analysis of Clocked Sequential Circuits

- State Table (Transition Table)

| Present State | Next State | | | | Output | |
|---|---|---|---|---|---|---|
| | $x = 0$ | | $x = 1$ | | $x = 0$ | $x = 1$ |
| $A$ $B$ | $A$ | $B$ | $A$ | $B$ | $y$ | $y$ |
| 0 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 1 | 0 | 0 | 1 | 0 | 1 | 0 |

$t$ $t+1$ $t$



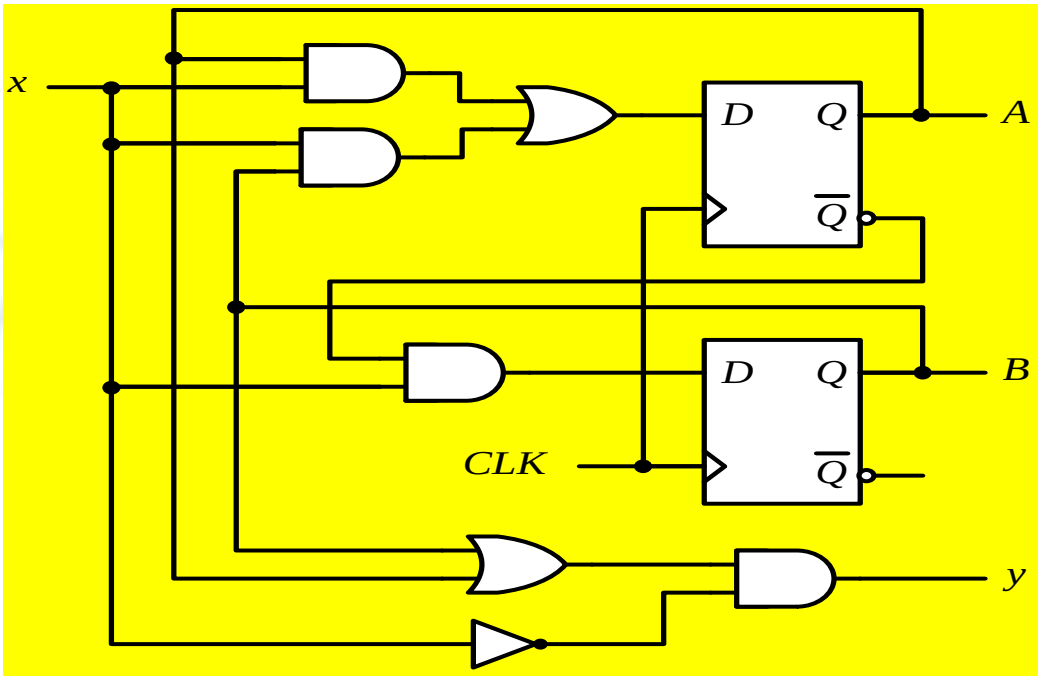

$$A(t+1) = A\,x + B\,x$$
$$B(t+1) = A'\,x$$
$$y(t) = (A + B)\,x'$$

# Analysis of Clocked Sequential Circuits

- State Table (Transition Table)

| Present State | | Next State | | | | Output | |
|---|---|---|---|---|---|---|---|
| | | $x = 0$ | | $x = 1$ | | $x = 0$ | $x = 1$ |
| $A$ | $B$ | $A$ | $B$ | $A$ | $B$ | $y$ | $y$ |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |

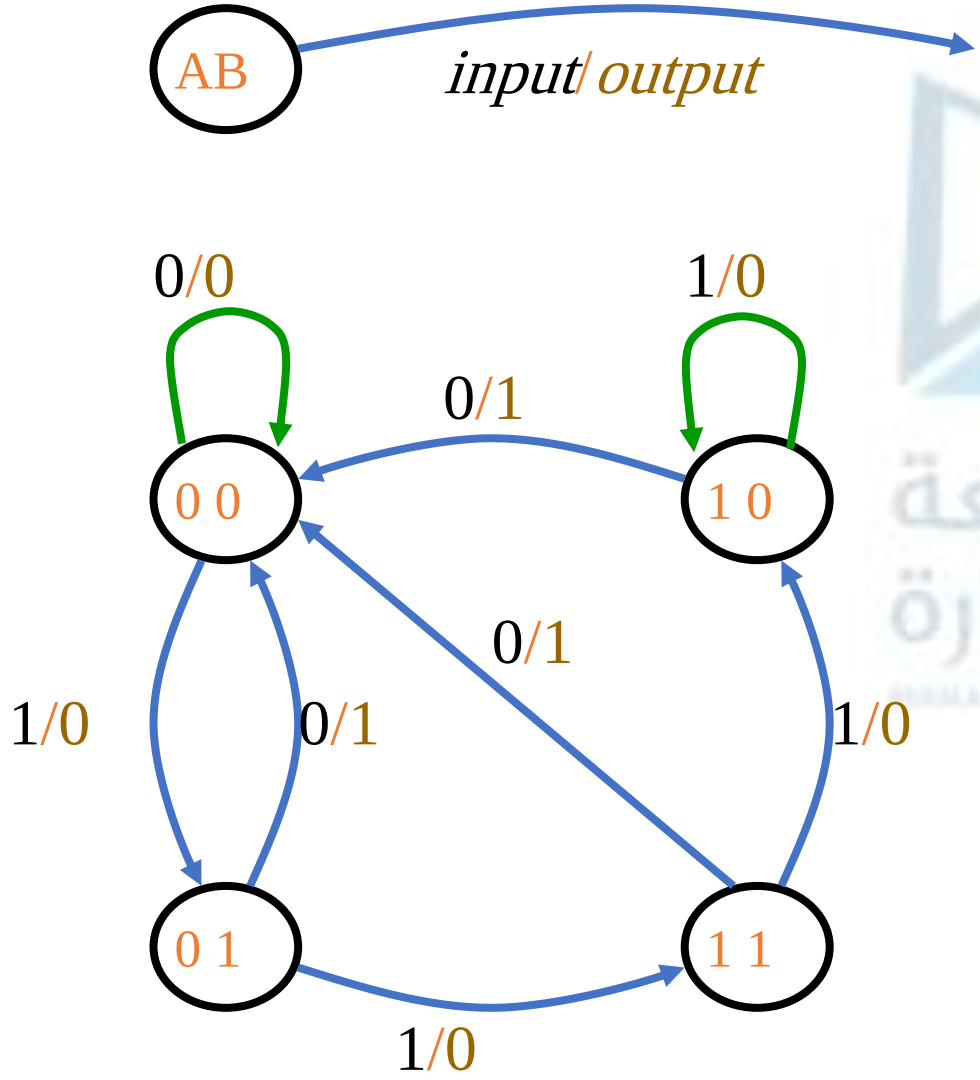
$t$ $t+1$ $t$



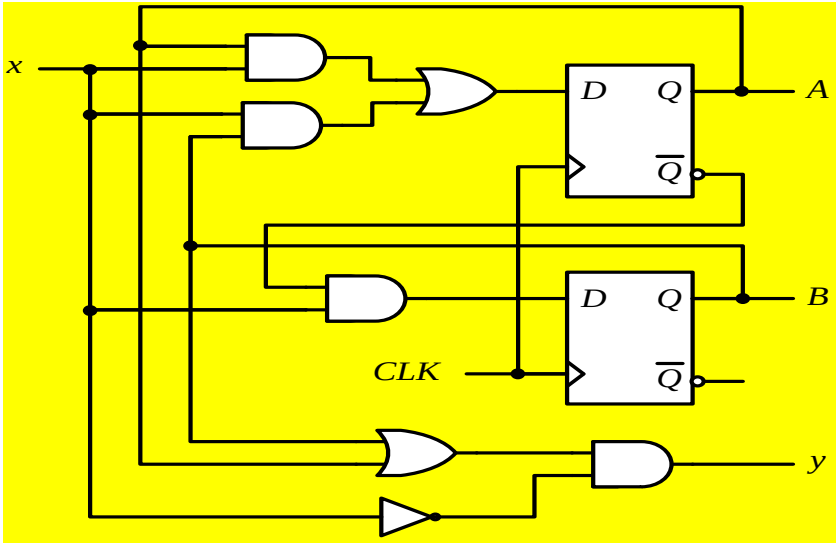

$$A(t+1) = A\,x + B\,x$$
$$B(t+1) = A'\,x$$
$$y(t) = (A + B)\,x'$$

# Analysis of Clocked Sequential Circuits

- State Diagram




| Present State | Next State | | | | Output | |
|---|---|---|---|---|---|---|
| | $x = 0$ | | $x = 1$ | | $x = 0$ | $x = 1$ |
| $A$ $B$ | $A$ | $B$ | $A$ | $B$ | $y$ | $y$ |
| 0 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 1 | 0 | 0 | 1 | 0 | 1 | 0 |

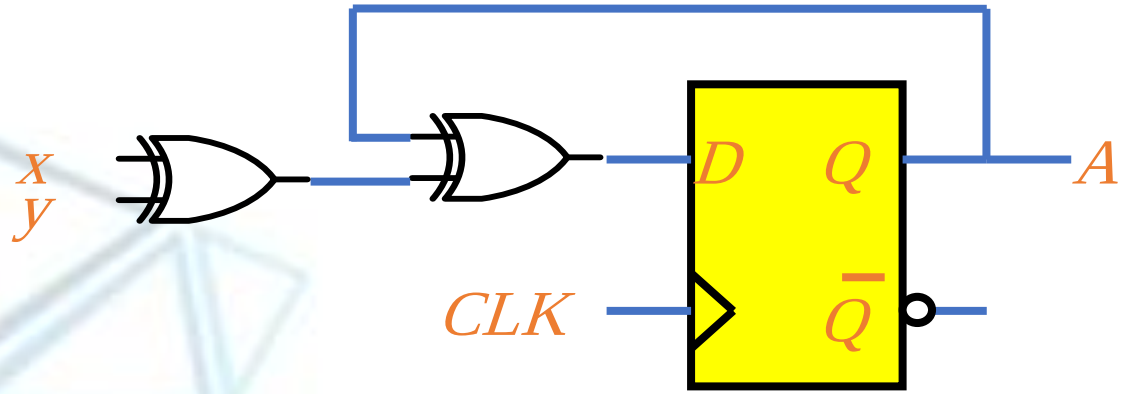


# Analysis of Clocked Sequential Circuits

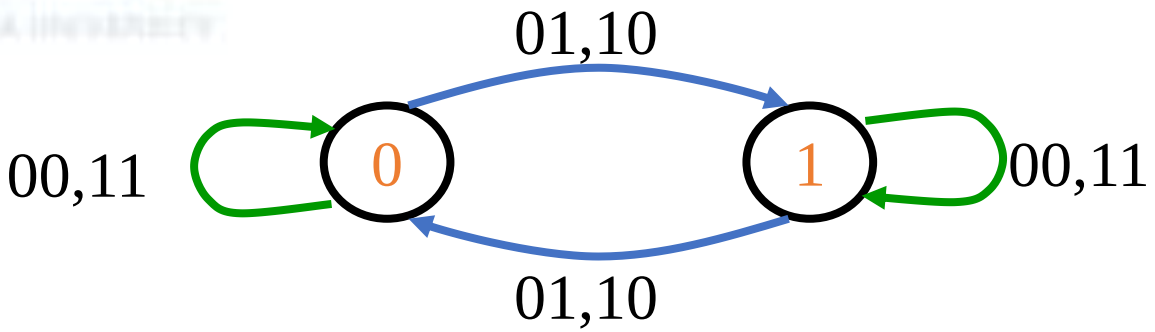
- *D* Flip-Flops

*Example*:

| Present State | Input | | Next State |
|---|---|---|---|
| *A* | *x* | *y* | *A* |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |




$$A(t+1) = D_A = A \oplus x \oplus y$$

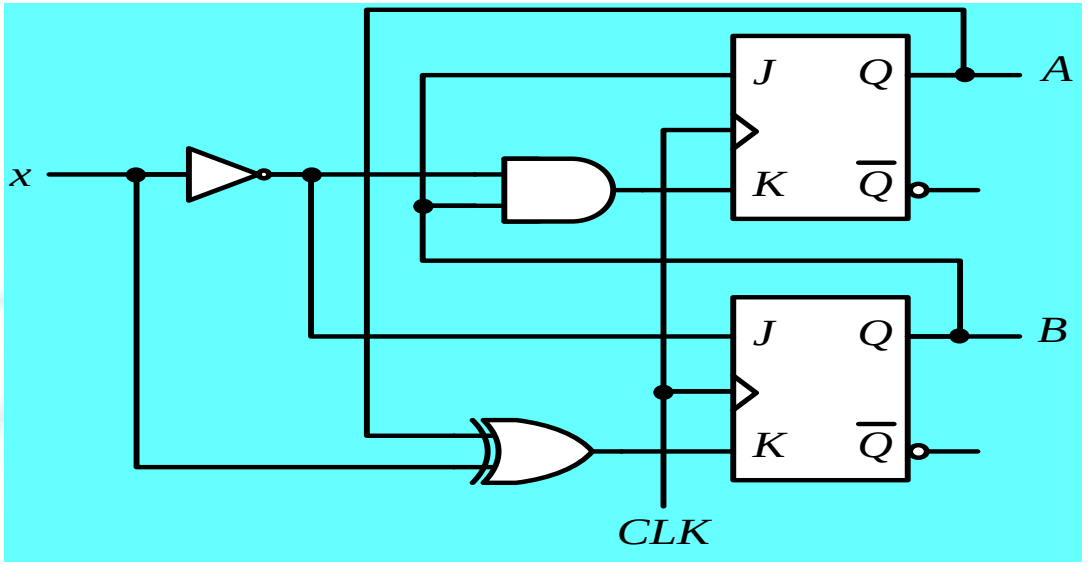


# Analysis of Clocked Sequential Circuits

- *JK* Flip-Flops

*Example*:

| Present State | | I/P | Next State | | Flip-Flop Inputs | | | |
|---|---|---|---|---|---|---|---|---|
| $A$ | $B$ | $x$ | $A$ | $B$ | $J_A$ | $K_A$ | $J_B$ | $K_B$ |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |




$J_A = B$ $\quad K_A = B\,x'$

$J_B = x'$ $\quad K_B = A \oplus x$

$$A(t+1) = J_A Q'_A + K'_A Q_A$$
$$= A'B + AB' + Ax$$

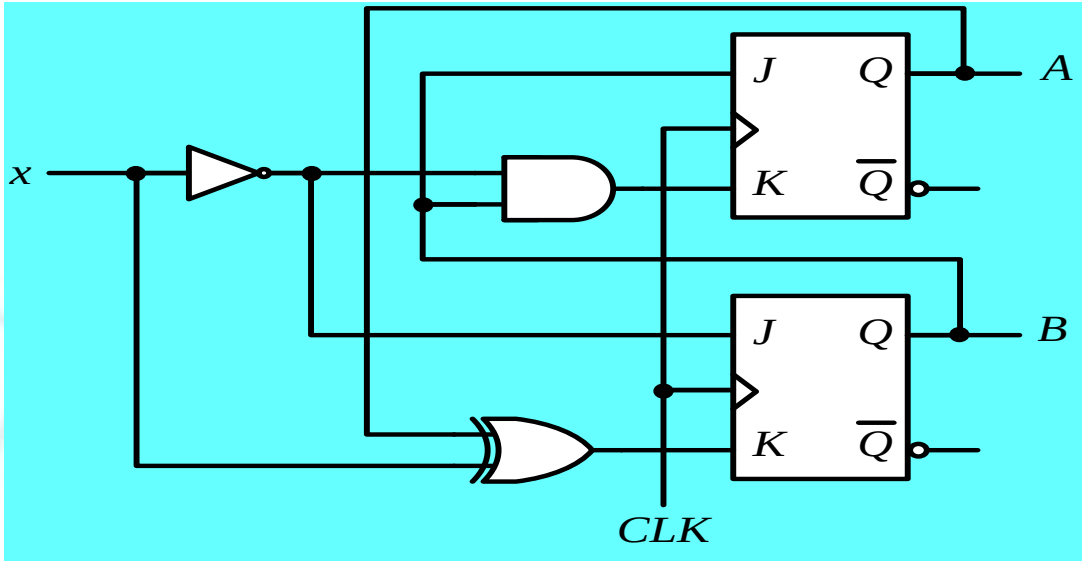
$$B(t+1) = J_B Q'_B + K'_B Q_B$$
$$= B'x' + ABx + A'Bx'$$

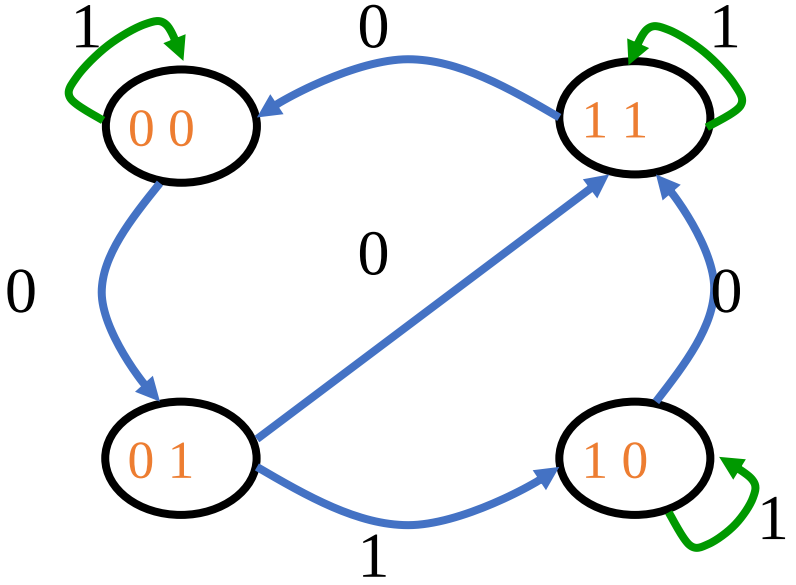
# Analysis of Clocked Sequential Circuits

- *JK* Flip-Flops

*Example*:

| Present State | | I/P | Next State | | Flip-Flop Inputs | | | |
|---|---|---|---|---|---|---|---|---|
| $A$ | $B$ | $x$ | $A$ | $B$ | $J_A$ | $K_A$ | $J_B$ | $K_B$ |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |



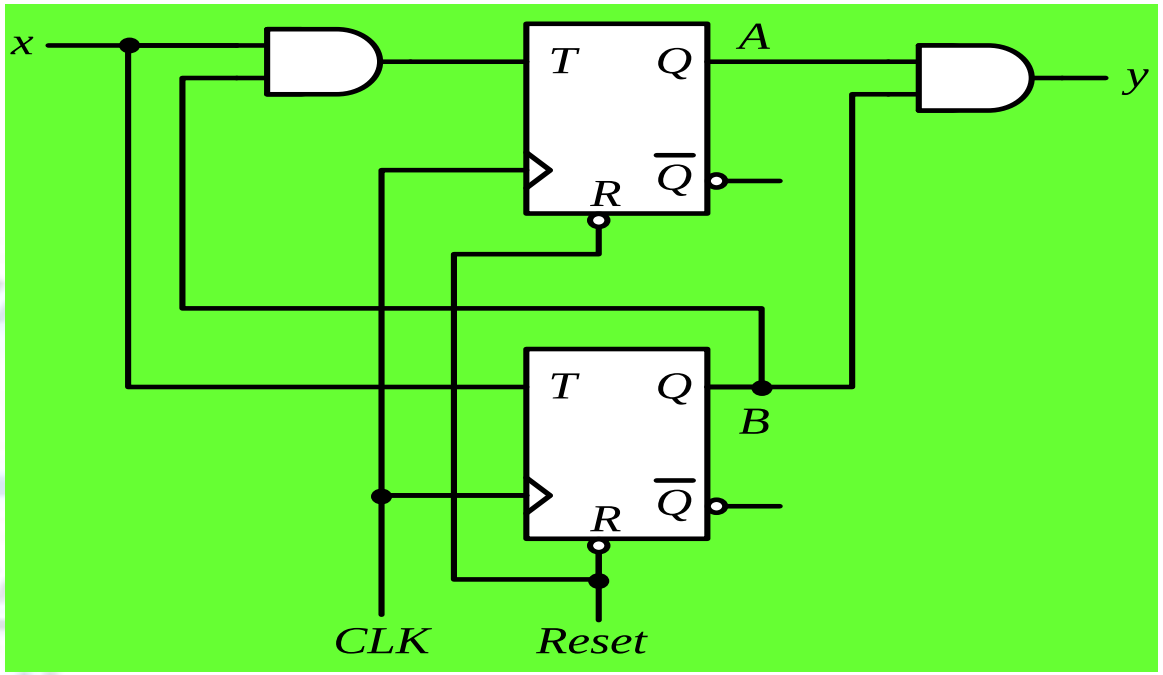



# Analysis of Clocked Sequential Circuits

- *T* Flip-Flops

*Example*:

| Present State | | I/P | Next State | | F.F Inputs | | O/P |
|---|---|---|---|---|---|---|---|
| *A* | *B* | *x* | *A* | *B* | $T_A$ | $T_B$ | *y* |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |




$$T_A = B\,x \qquad T_B = x$$

$$y = A\,B$$

$$A(t+1) = T_A Q'_A + T'_A Q_A$$
$$= AB' + Ax' + A'Bx$$

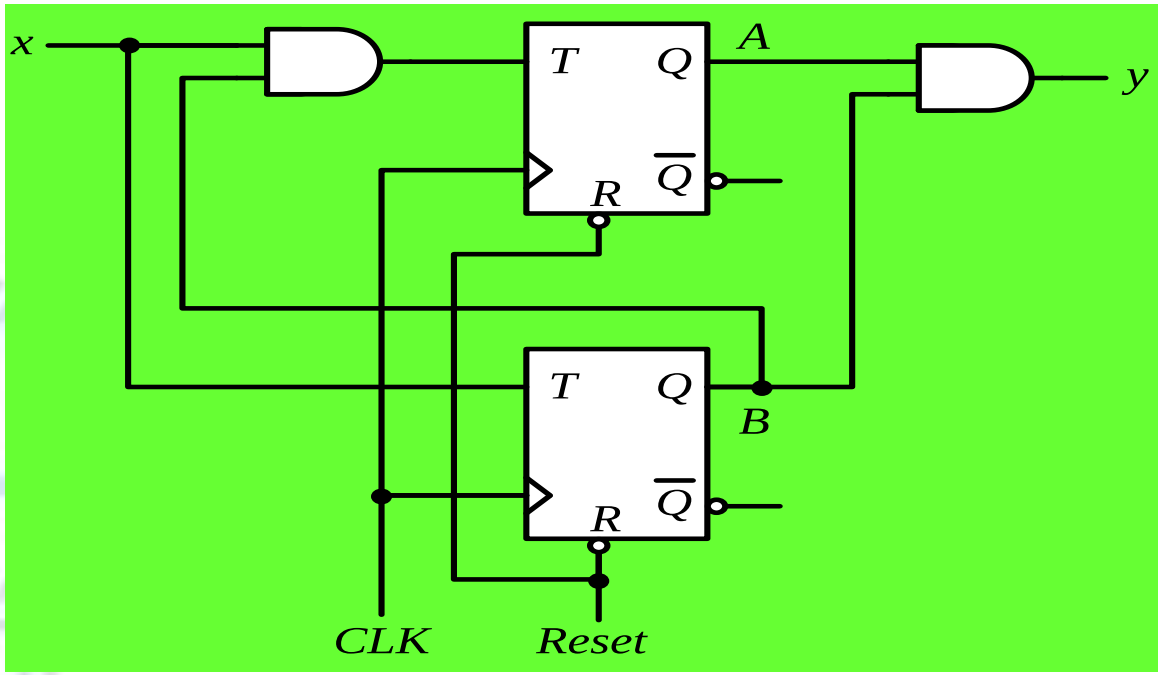
$$B(t+1) = T_B Q'_B + T'_B Q_B$$
$$= x \oplus B$$

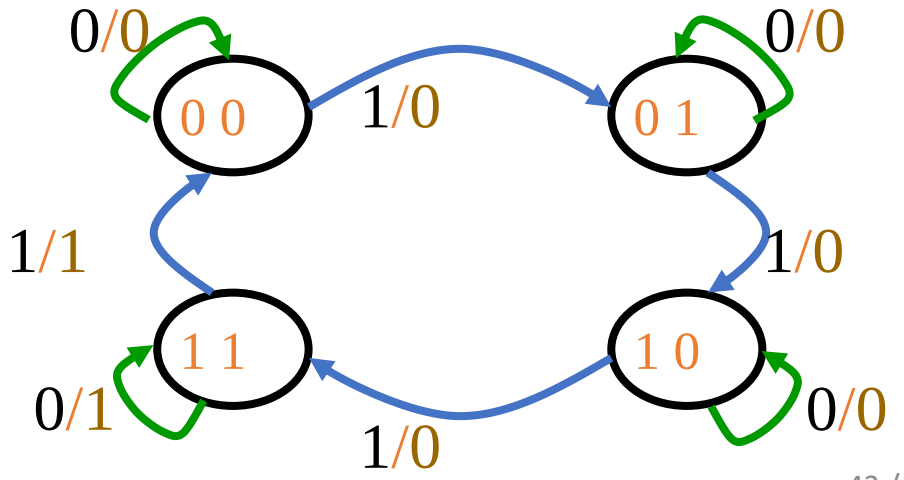
# Analysis of Clocked Sequential Circuits

- *T* Flip-Flops

*Example*:

| Present State | | I/P | Next State | | F.F Inputs | | O/P |
|---|---|---|---|---|---|---|---|
| *A* | *B* | *x* | *A* | *B* | $T_A$ | $T_B$ | *y* |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |



# Mealy and Moore Models

## *Mealy*

| Present State | | I/P | Next State | | O/P |
|---|---|---|---|---|---|
| *A* | *B* | *x* | *A* | *B* | *y* |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 |

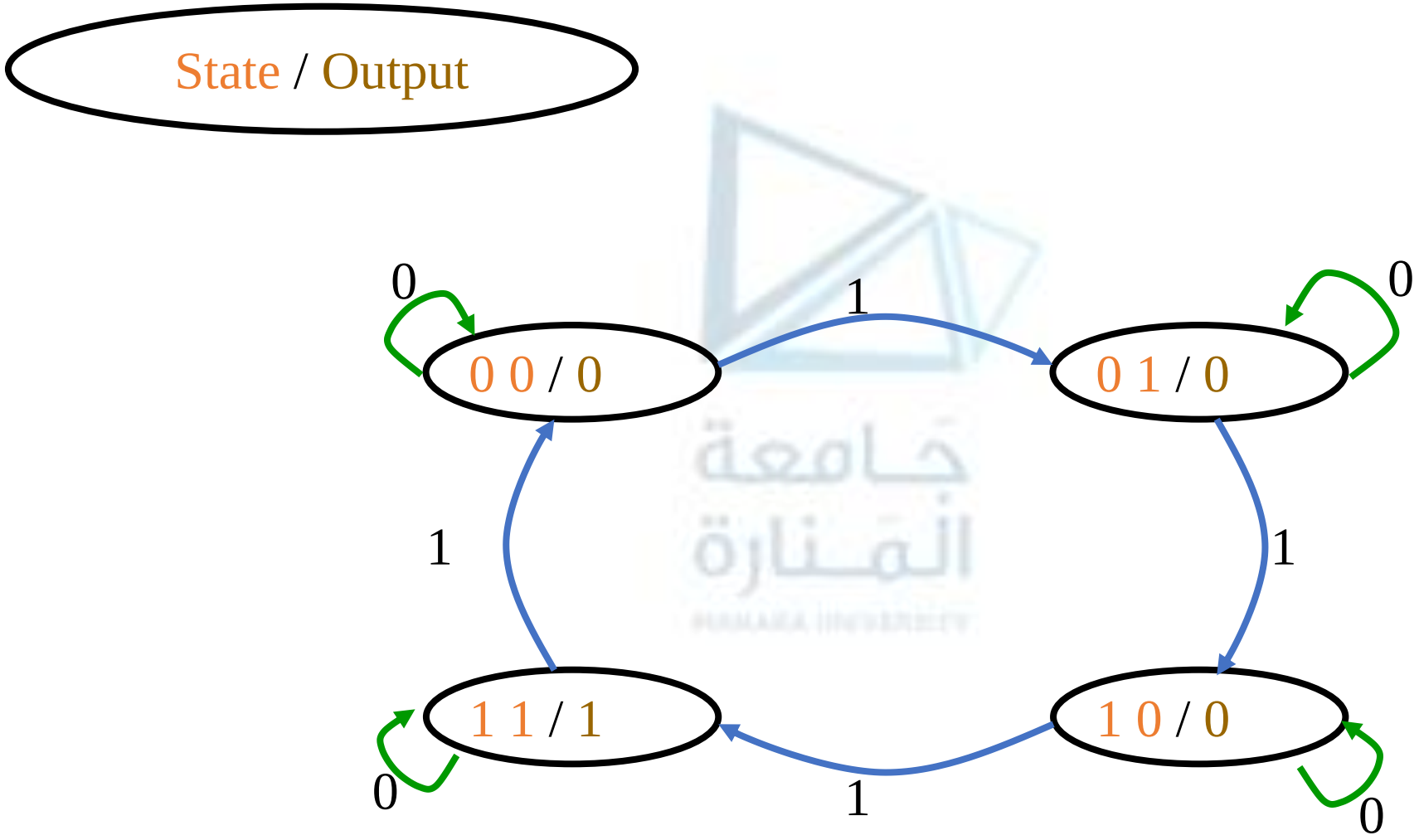
*For the same state,*
*the output changes with the input*

## *Moore*

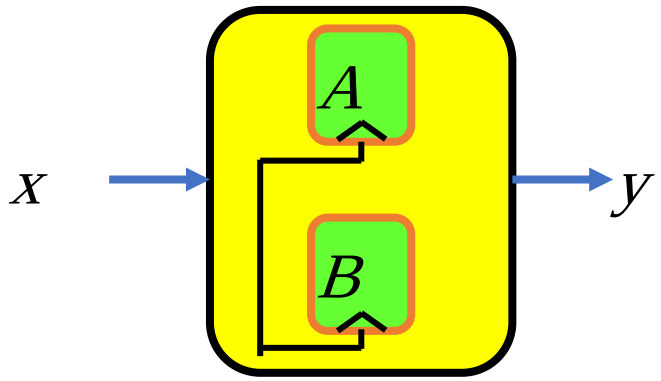
| Present State | | I/P | Next State | | O/P |
|---|---|---|---|---|---|
| *A* | *B* | *x* | *A* | *B* | *y* |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 |

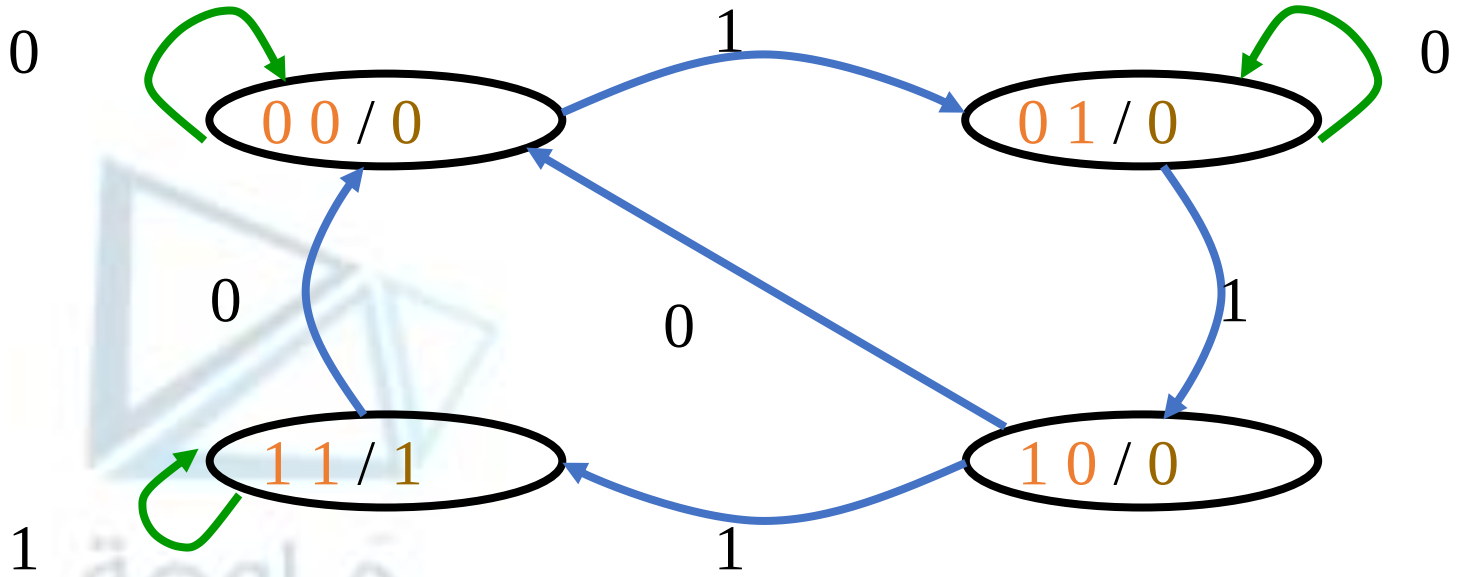
*For the same state,*
*the output does not change with the input*

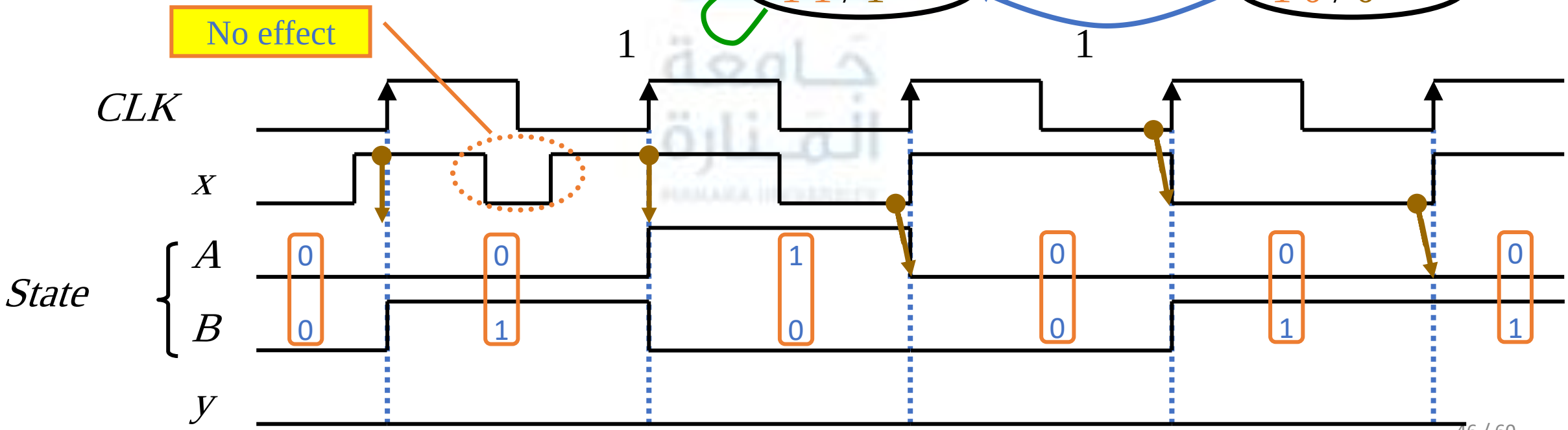
# Moore State Diagram



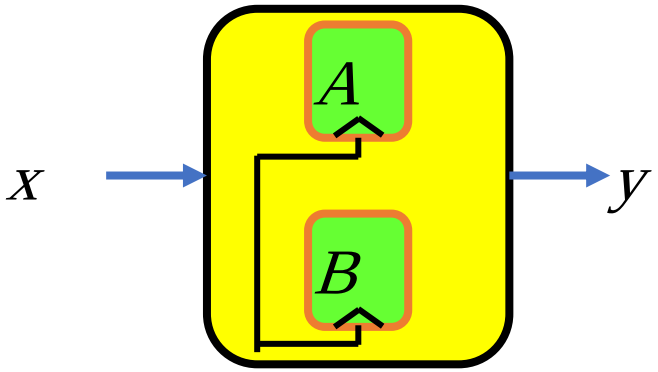
# Timing Diagram

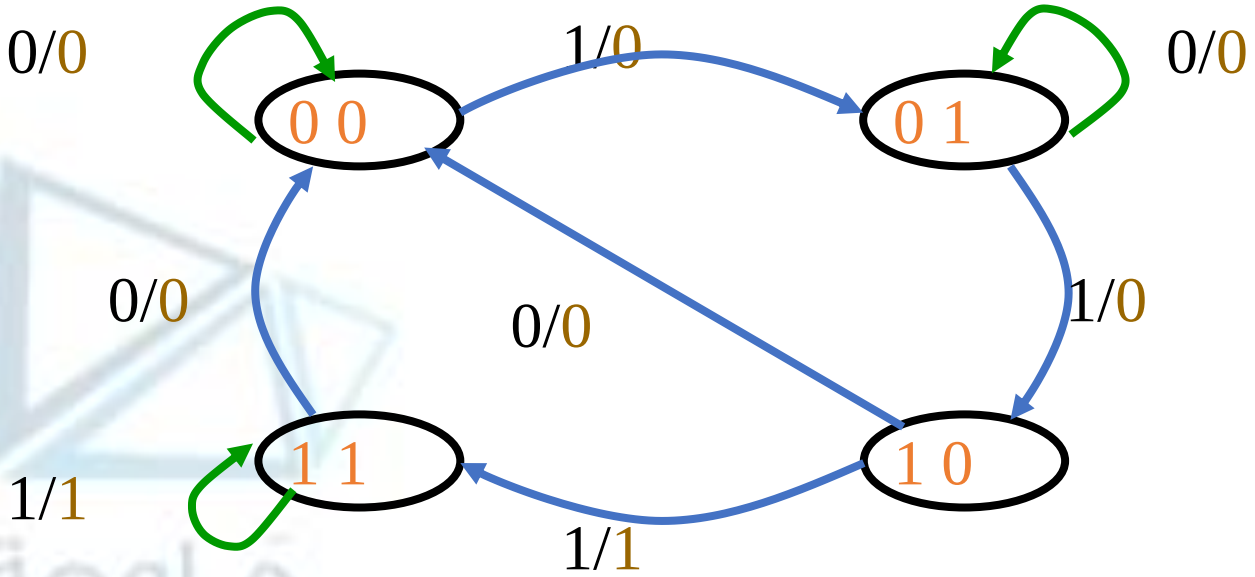


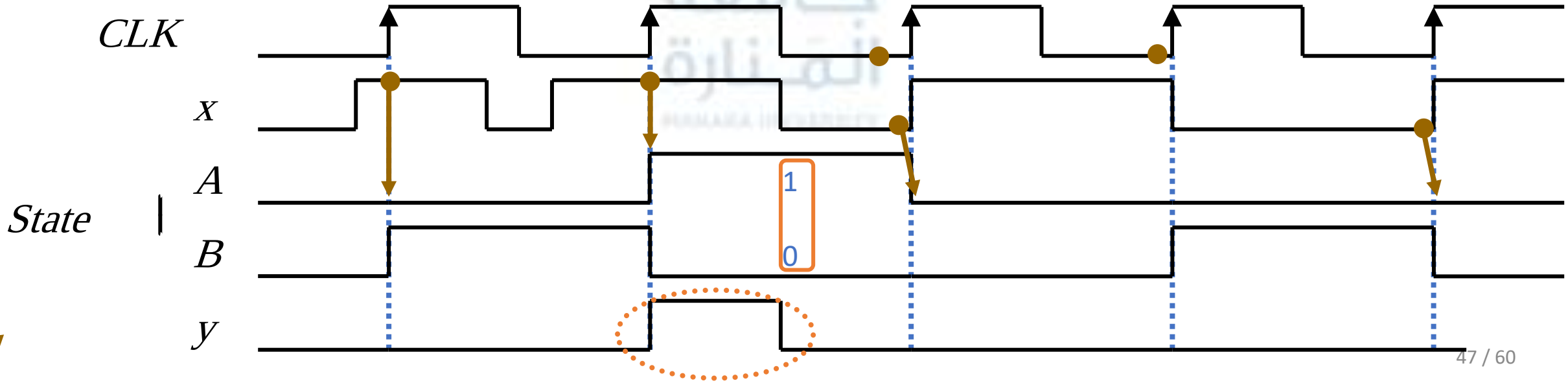



# Timing Diagram



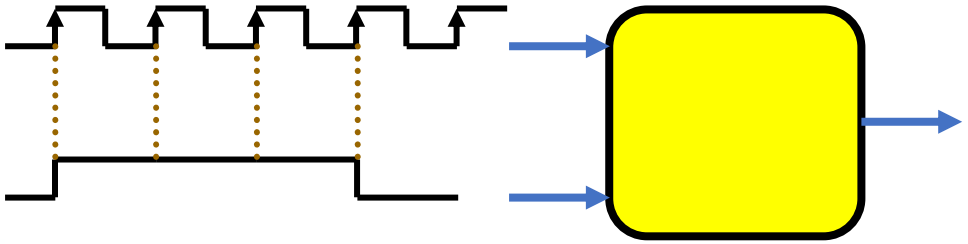



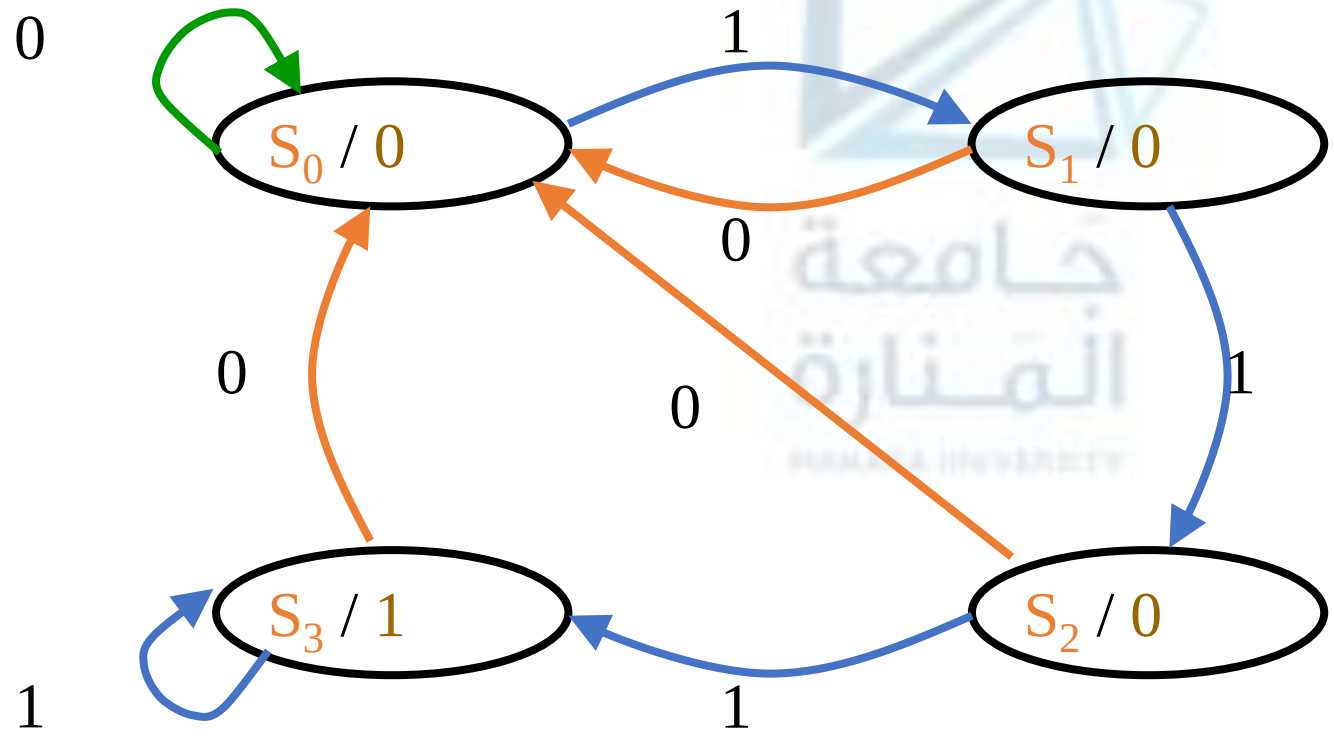



# Design of Clocked Sequential Circuits

- *Example*:

Detect 3 or more consecutive 1's





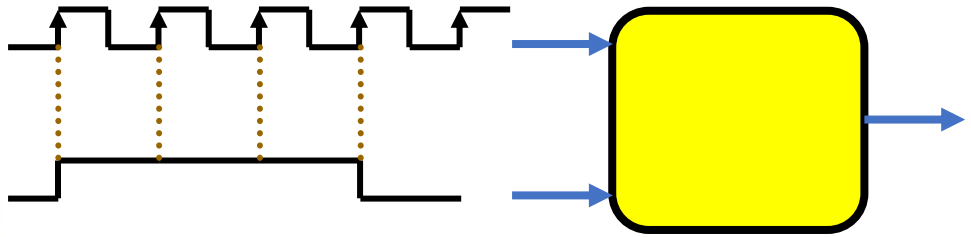

| State | *A B* |
|---|---|
| $S_0$ | 0 0 |
| $S_1$ | 0 1 |
| $S_2$ | 1 0 |
| $S_3$ | 1 1 |

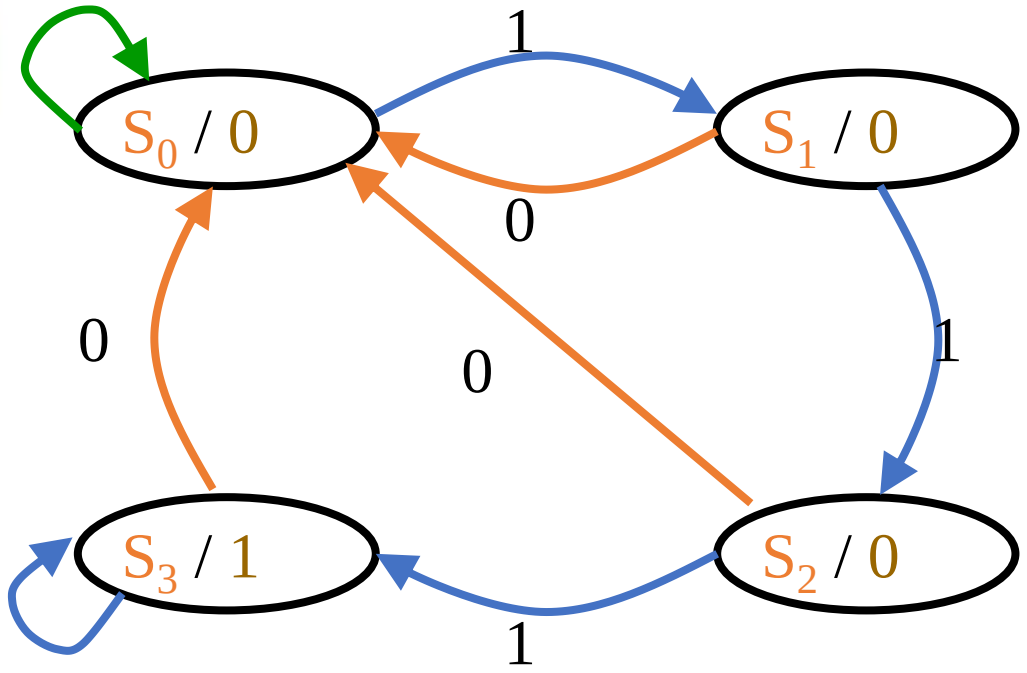
# Design of Clocked Sequential Circuits

- *Example*:

Detect 3 or more consecutive 1's

| Present State | | Input | Next State | | Output |
|---|---|---|---|---|---|
| *A* | *B* | *x* | *A* | *B* | *y* |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 |

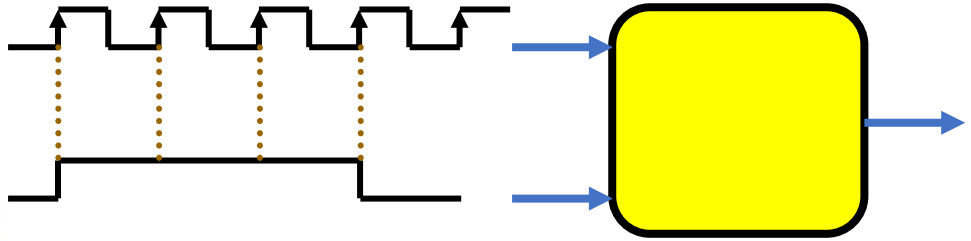




# Design of Clocked Sequential Circuits

- *Example*:

Detect 3 or more consecutive 1's



| Present State | | Input | Next State | | Output |
|---|---|---|---|---|---|
| *A* | *B* | *x* | *A* | *B* | *y* |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 |

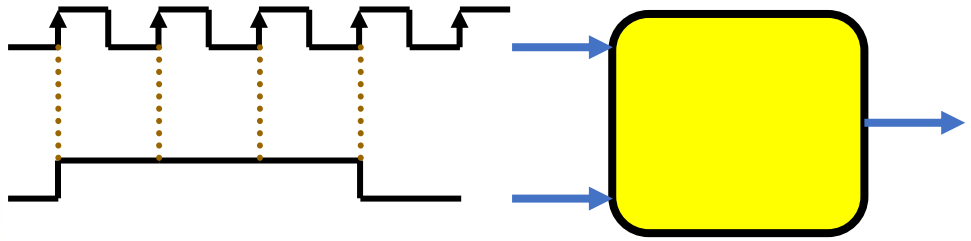
Synthesis using *D* Flip-Flops

$$A(t+1) = D_A(A, B, x)$$
$$= \sum(3, 5, 7)$$
$$B(t+1) = D_B(A, B, x)$$
$$= \sum(1, 5, 7)$$
$$y(A, B, x) = \sum(6, 7)$$

# Design of Clocked Sequential Circuits with *D* F.F.

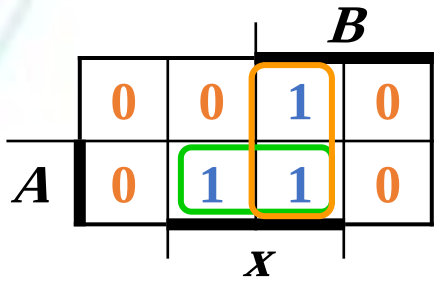
- *Example*:

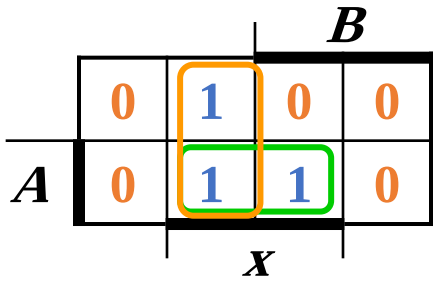
Detect 3 or more consecutive 1's

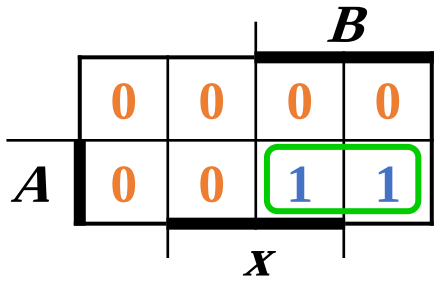


Synthesis using *D* Flip-Flops

$$D_A(A, B, x) = \sum(3, 5, 7)$$
$$= A\,x + B\,x$$
$$D_B(A, B, x) = \sum(1, 5, 7)$$
$$= A\,x + B'x$$
$$y(A, B, x) = \sum(6, 7)$$
$$= A\,B$$



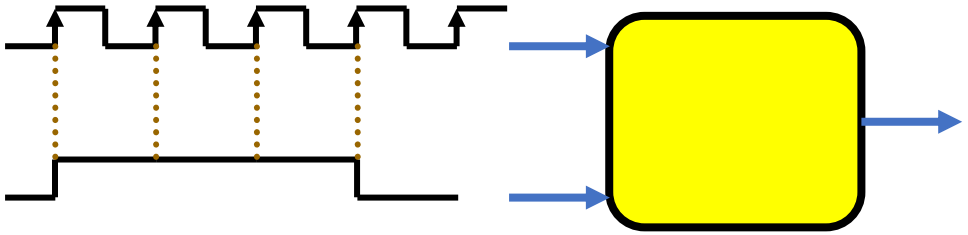



# Design of Clocked Sequential Circuits with *D* F.F.

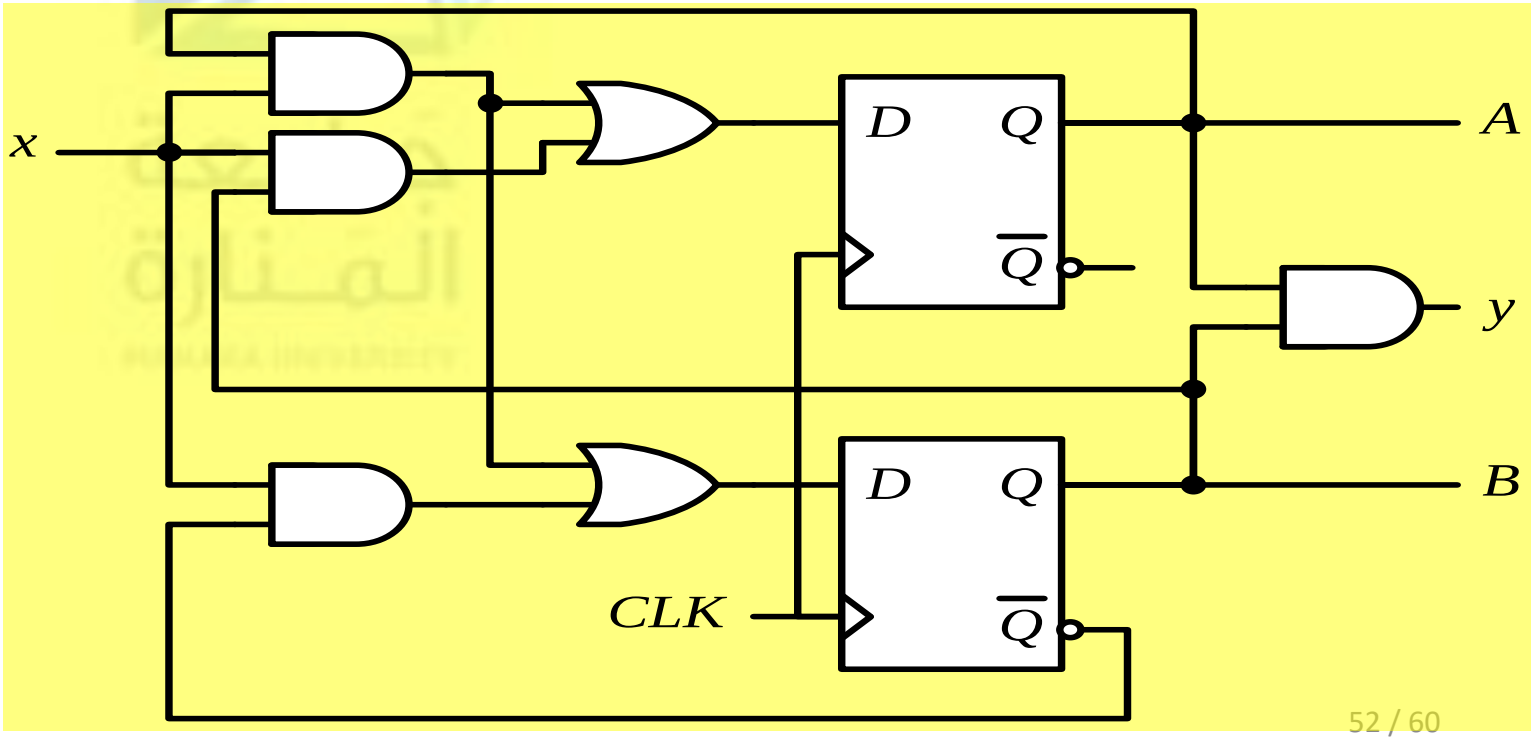
- *Example*:

Detect 3 or more consecutive 1's



Synthesis using *D* Flip-Flops

$$D_A = A\,x + B\,x$$
$$D_B = A\,x + B'x$$
$$y = A\,B$$



# Flip-Flop Excitation Tables

| Present State | Next State | F.F. Input |
|---|---|---|
| $Q(t)$ | $Q(t+1)$ | $D$ |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

| Present State | Next State | F.F. Input | |
|---|---|---|---|
| $Q(t)$ | $Q(t+1)$ | $J$ | $K$ |
| 0 | 0 | 0 | x |
| 0 | 1 | 1 | x |
| 1 | 0 | x | 1 |
| 1 | 1 | x | 0 |

0 0 (No change)
0 1 (Reset)

1 0 (Set)
1 1 (Toggle)

0 1 (Reset)
1 1 (Toggle)

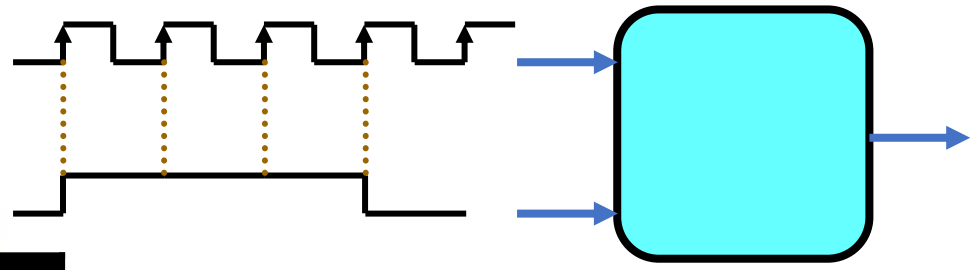
0 0 (No change)
1 0 (Set)

| $Q(t)$ | $Q(t+1)$ | $T$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

# Design of Clocked Sequential Circuits with *JK* F.F.

- *Example*:

Detect 3 or more consecutive 1's



| Present State | | Input | Next State | | Flip-Flop Inputs | | | |
|---|---|---|---|---|---|---|---|---|
| $Q$ | $B$ | $x$ | $A$ | $B$ | $J_A$ | $K_A$ | $J_B$ | $K_B$ |
| 0 | 0 | 0 | 0 | 0 | 0 | x | 0 | x |
| 0 | 0 | 1 | 0 | 1 | 0 | x | 1 | x |
| 0 | 1 | 0 | 0 | 0 | 0 | x | x | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | x | x | 1 |
| 1 | 0 | 0 | 0 | 0 | x | 1 | 0 | x |
| 1 | 0 | 1 | 1 | 1 | x | 0 | 1 | x |
| 1 | 1 | 0 | 0 | 0 | x | 1 | x | 1 |
| 1 | 1 | 1 | 1 | 1 | x | 0 | x | 0 |

Synthesis using *JK* F.F.

$J_A(A, B, x) = \sum(3)$

$d_{JA}(A, B, x) = \sum(4,5,6,7)$

$K_A(A, B, x) = \sum(4, 6)$

$d_{KA}(A, B, x) = \sum(0,1,2,3)$

$J_B(A, B, x) = \sum(1, 5)$

$d_{JB}(A, B, x) = \sum(2,3,6,7)$

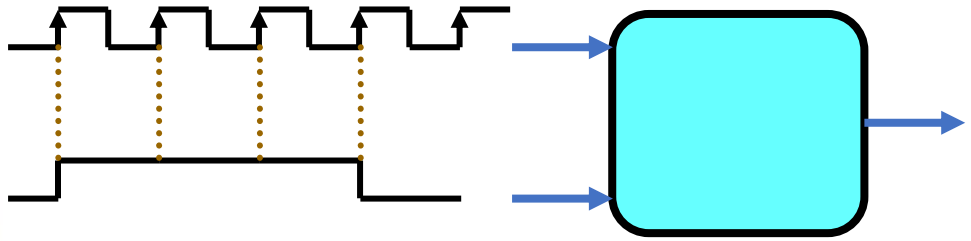
$K_B(A, B, x) = \sum(2, 3, 6)$

$d_{KB}(A, B, x) = \sum(0,1,4,5)$

# Design of Clocked Sequential Circuits with *JK* F.F.

- *Example*:

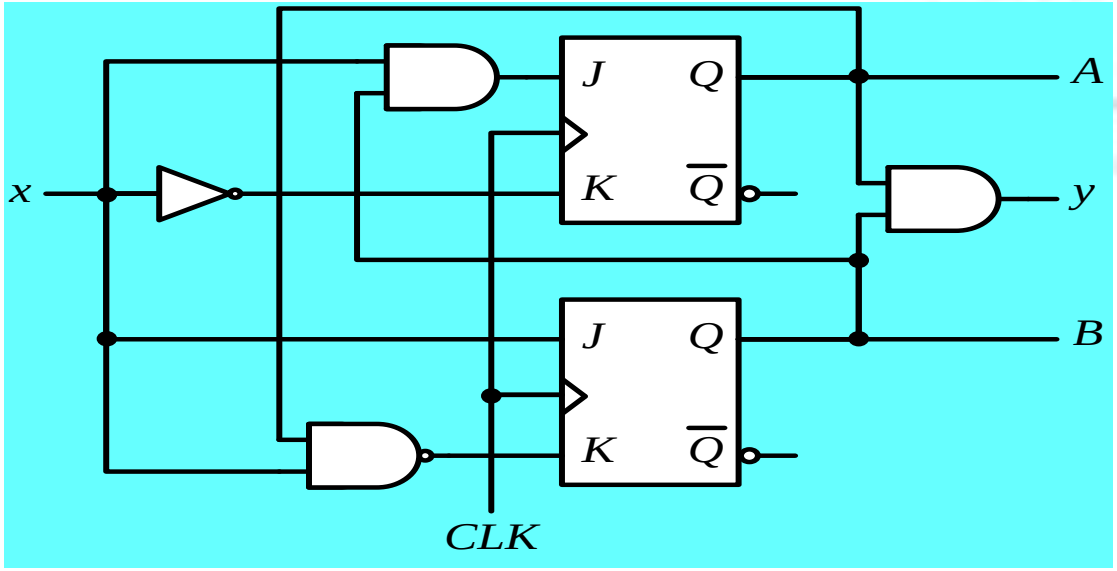
Detect 3 or more consecutive 1's

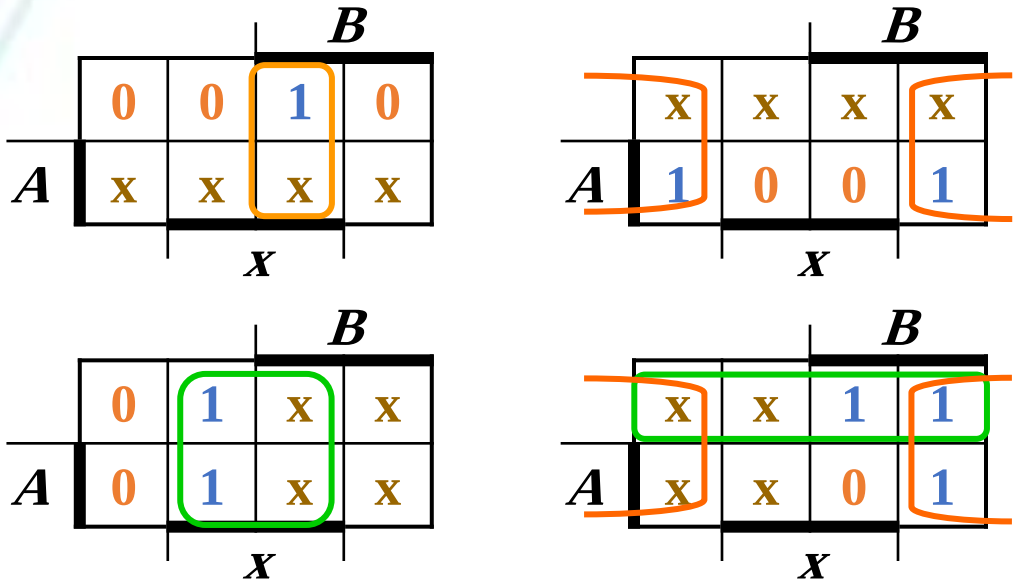


Synthesis using *JK* Flip-Flops

$J_A = B\,x \qquad K_A = x'$

$J_B = x \qquad K_B = A' + x'$

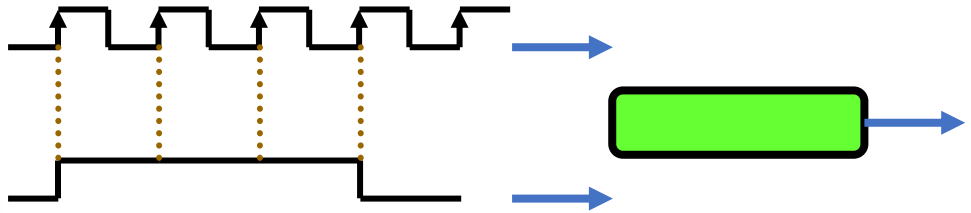


# Design of Clocked Sequential Circuits with *T* F.F.

- *Example*:

Detect 3 or more consecutive 1's



| Present State | | Input | Next State | | F.F. Input | |
|---|---|---|---|---|---|---|
| $A$ | $B$ | $x$ | $A$ | $B$ | $T_A$ | $T_B$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 |

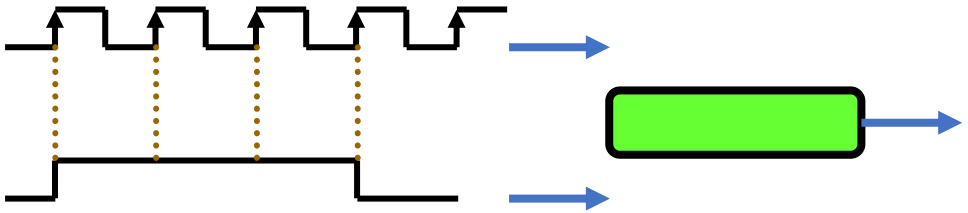
Synthesis using *T* Flip-Flops

$$T_A(A, B, x) = \sum(3, 4, 6)$$
$$T_B(A, B, x) = \sum(1, 2, 3, 5, 6)$$

# Design of Clocked Sequential Circuits with *T* F.F.

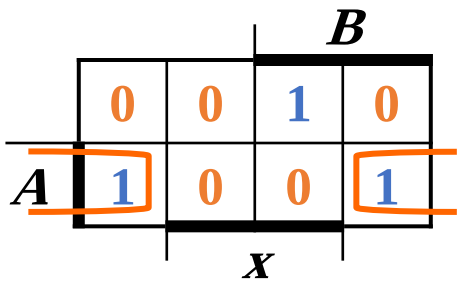
- *Example*:

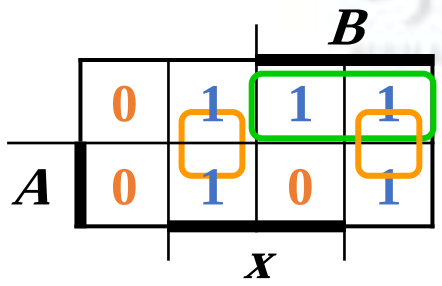
Detect 3 or more consecutive 1's

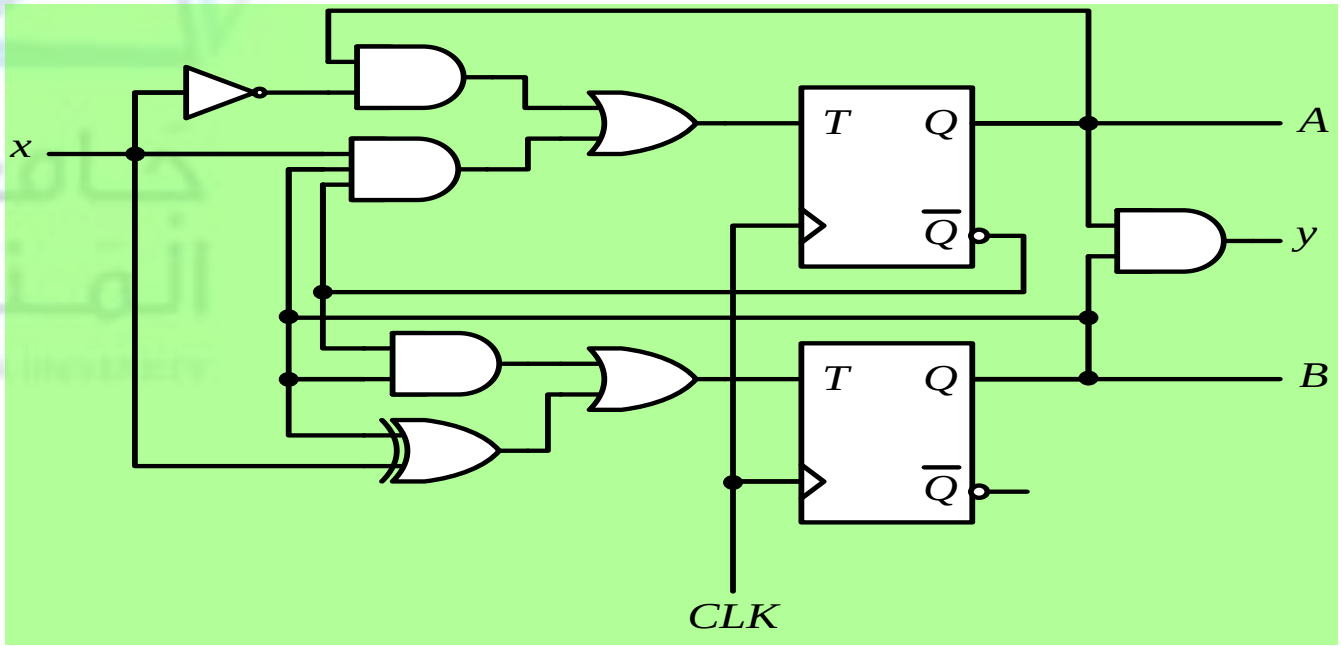


Synthesis using *T* Flip-Flops

$$T_A = A\,x' + A'B\,x$$
$$T_B = A'B + B \oplus x$$



# Homework

- Mano
  - Chapter 5
    - 5-1
    - 5-3
    - 5-6
    - 5-8
    - 5-9

# Homework

**5-1** **The *D* latch is constructed with four NAND gates and an inverter. Consider the following three other ways for obtaining a *D* latch. In each case, draw the logic diagram and verify the circuit operation.**

**(a) Use NOR gates for the *SR* latch part and AND gates for the other two. An inverter may be needed.**

**(b) Use NOR gates for all four gates. Inverters may be needed.**

**(c) Use four NAND gates only (without an inverter). This can be done by connecting the output of the upper gate that goes to the *SR* latch to the input of the lower gate instead of the inverter output.**

# Homework

**5-3** **Show that the characteristic equation for the complement output of a *JK* flip-flop is**

$$Q'(t+1) = J'Q + KQ$$

**5-6** **A sequential circuit with two *D* flip-flops, *A* and *B*; two inputs, *x* and *y*; and one output, *z*, is specified by the following next-state and output equations:**

$$A(t+1) = x'y + xA$$
$$B(t+1) = x'B + xA$$
$$z = B$$

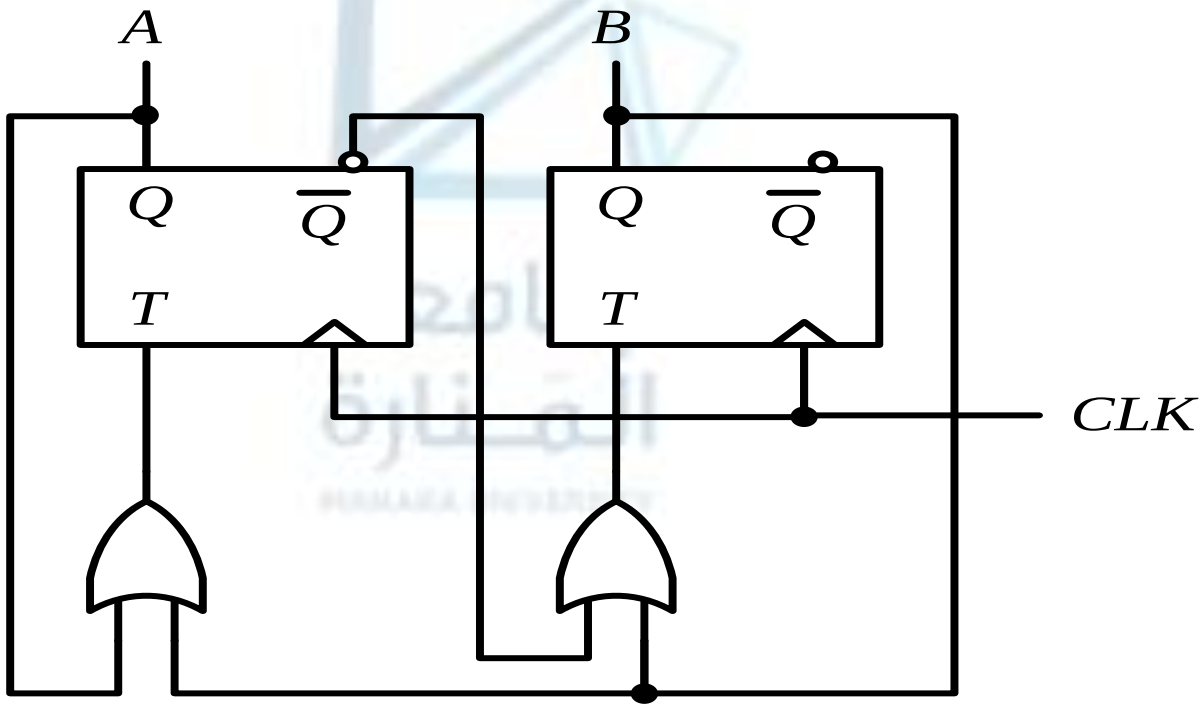
**(a) Draw the logic diagram of the circuit.**

**(b) List the state table for the sequential circuit.**

**(c) Draw the corresponding state diagram.**

# Homework

**5-8** **Derive the state table and the state diagram of the sequential shown circuit. Explain the function that the circuit performs.**



# Homework

**5-9** **A sequential circuit has two *JK* flip-flops *A* and *B* and one input *x*. The circuit is described by the following flip-flop input equations:**

$$J_A = x \qquad K_A = B'$$

$$J_B = x \qquad K_B = A$$

**(a) Derive the state equations $A(t+1)$ and $B(t+1)$ by substituting the input equations for the *J* and *K* variables.**

**(b) Draw the state diagram of the circuit.**