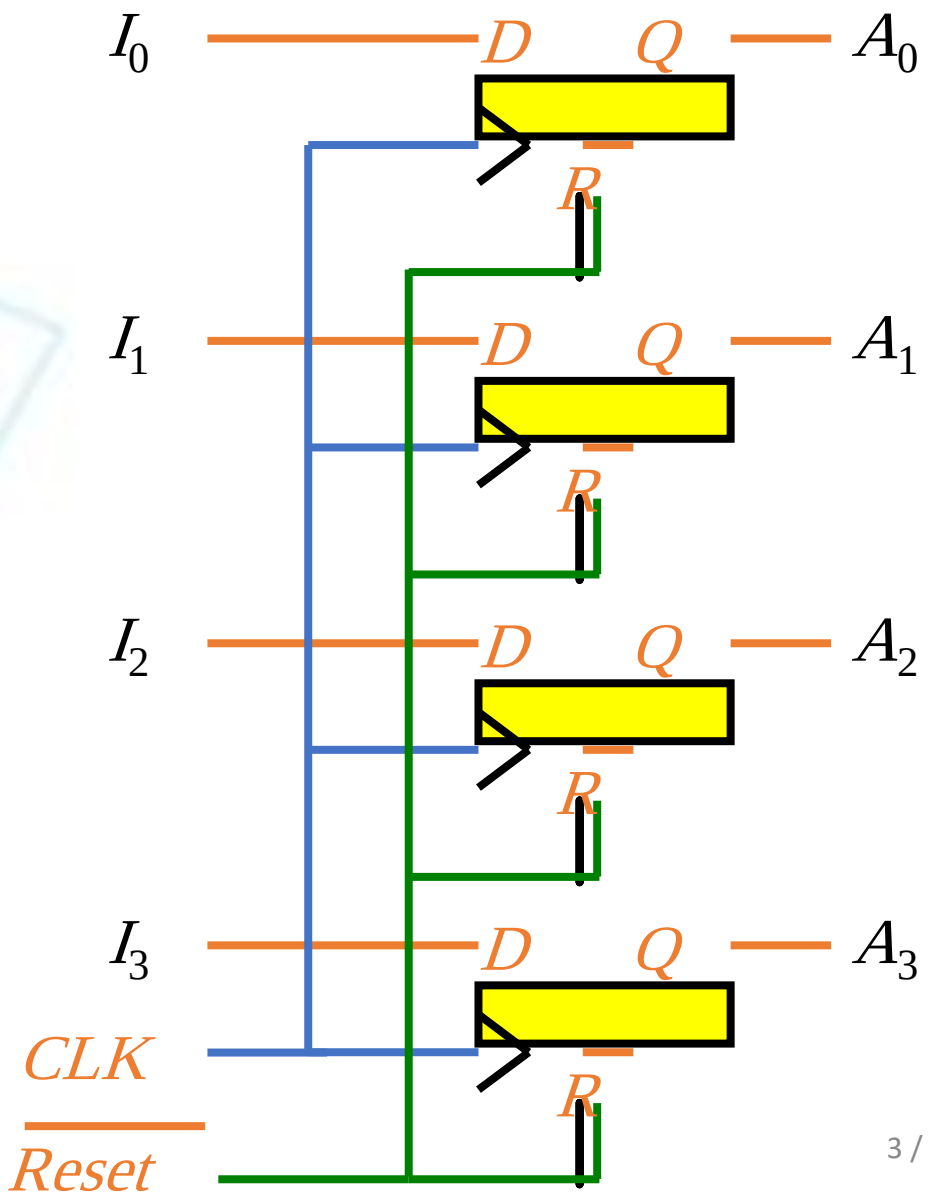
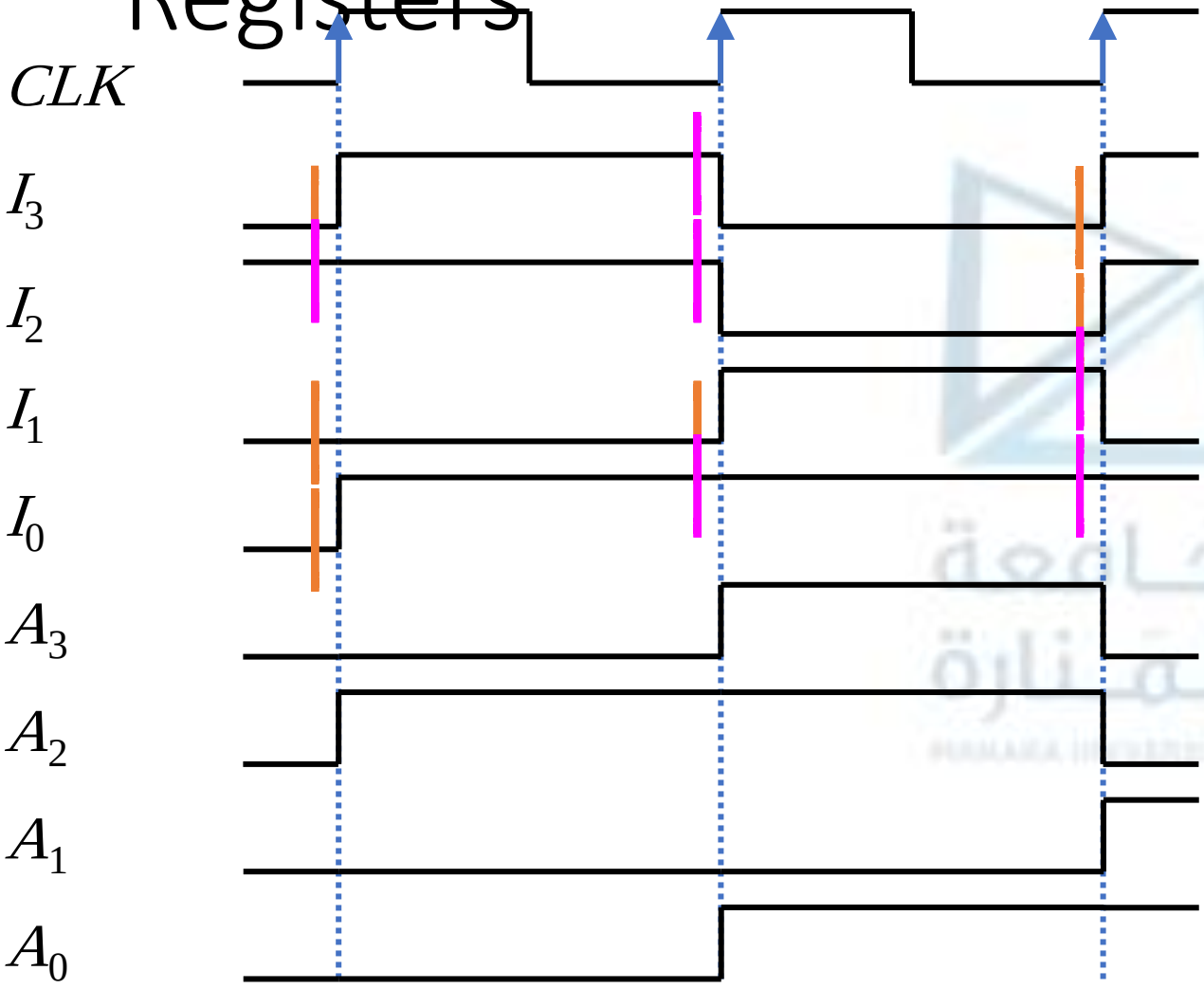
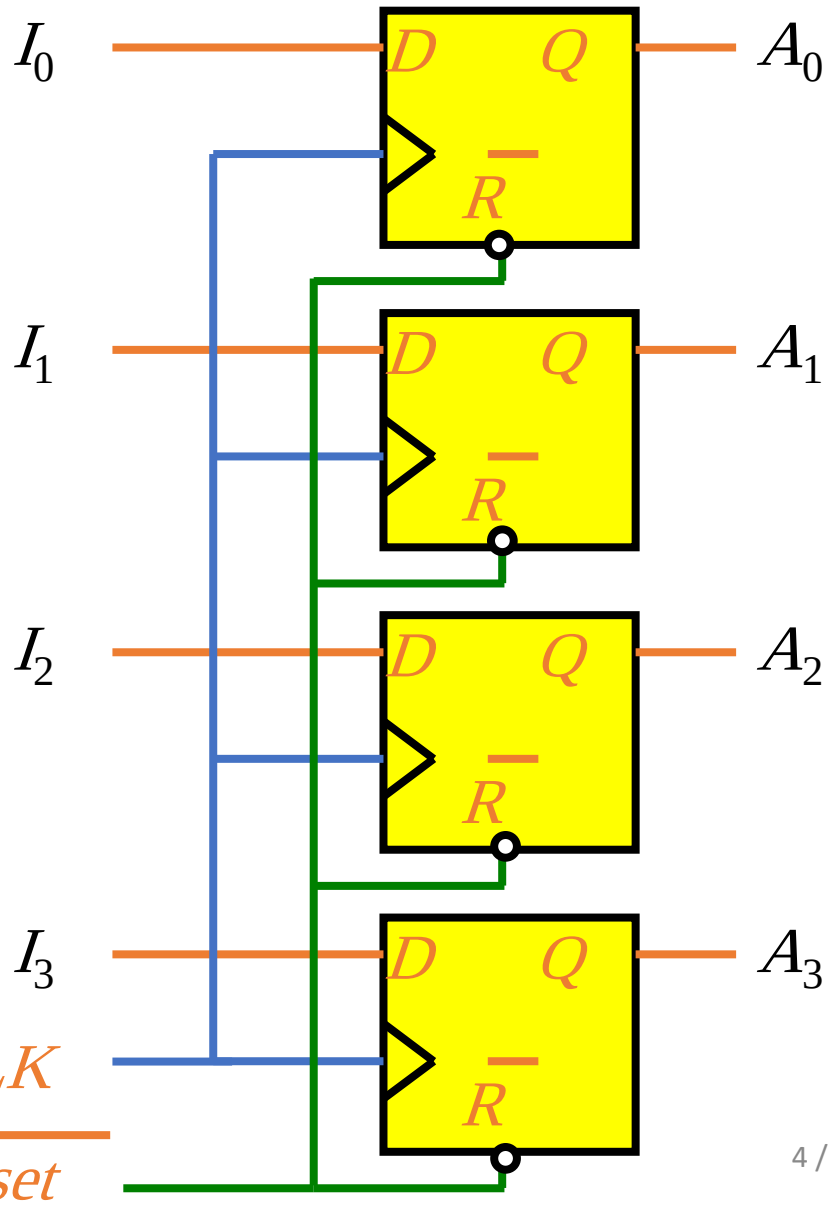
Registers

- Group of *D* Flip-Flops
- Synchronized (Single Clock)
- Store Data



Registers

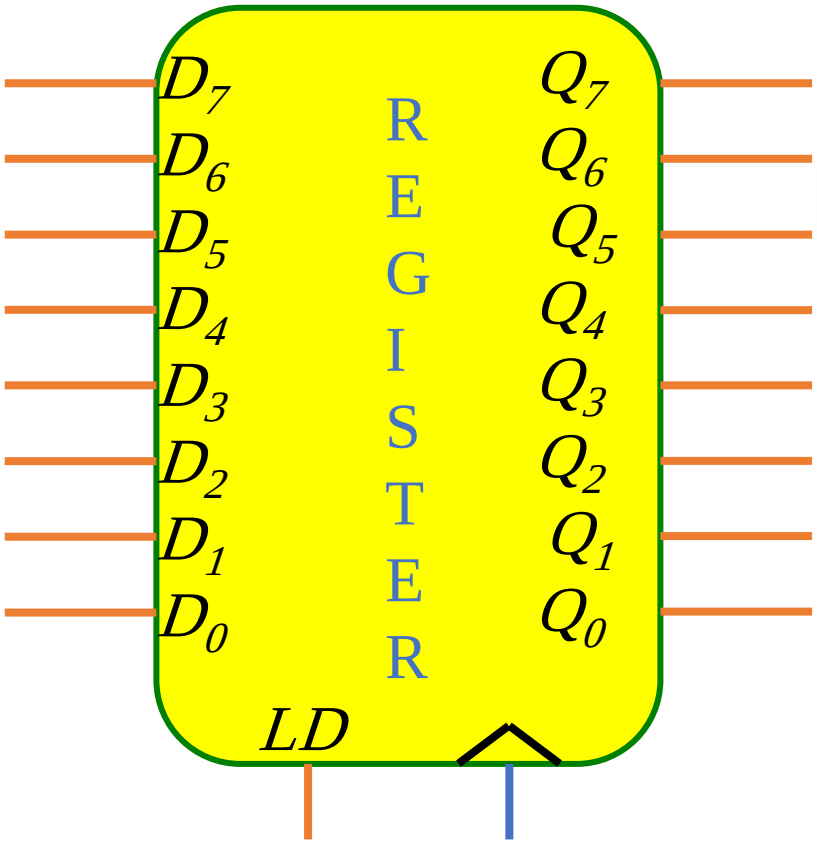




Note: New data has to go in with every clock

Registers with Parallel Load

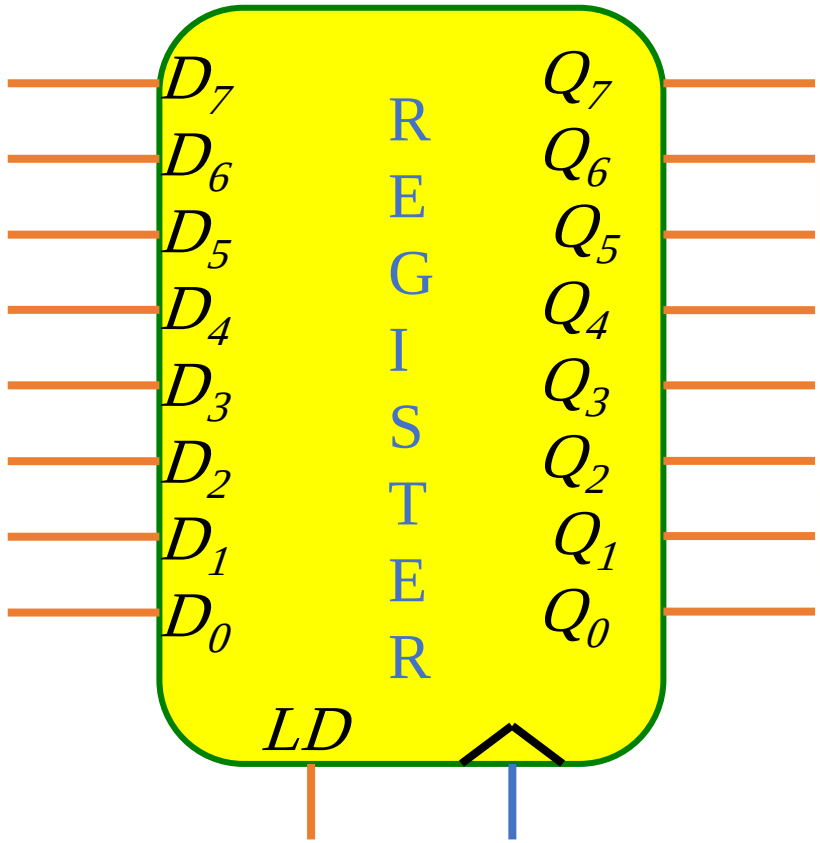
- Control *Loading* the Register with New Data

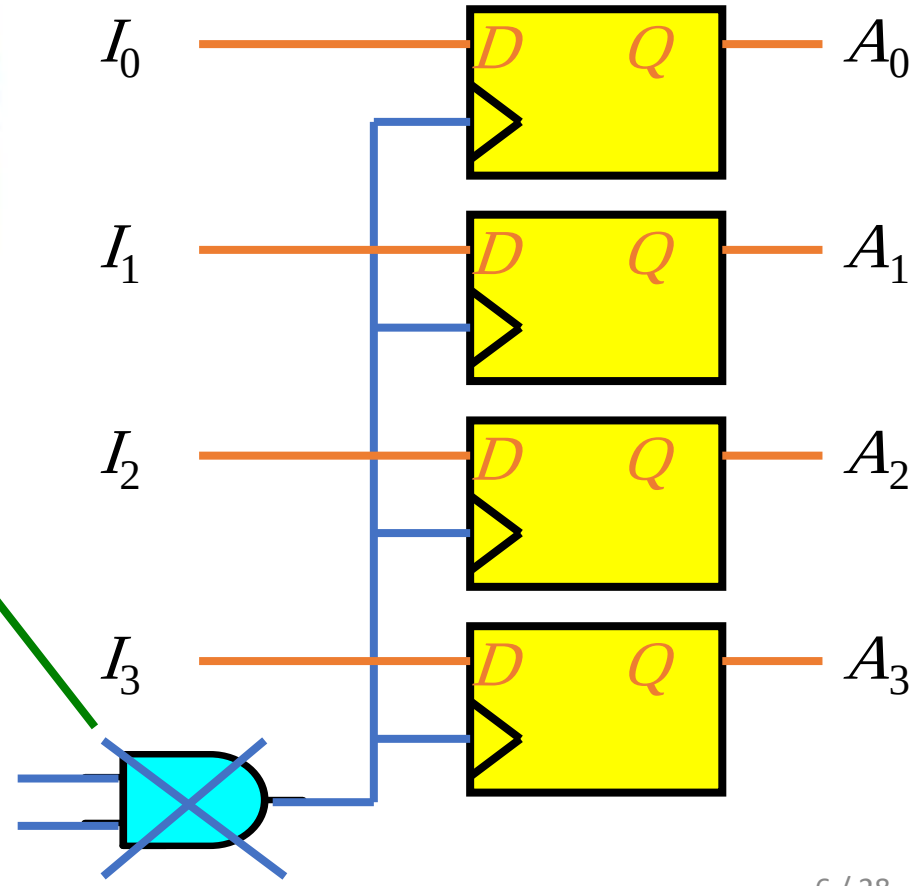


LD	*Q*(*t*+1)
0	*Q*(*t*)
1	*D*

Registers with Parallel Load

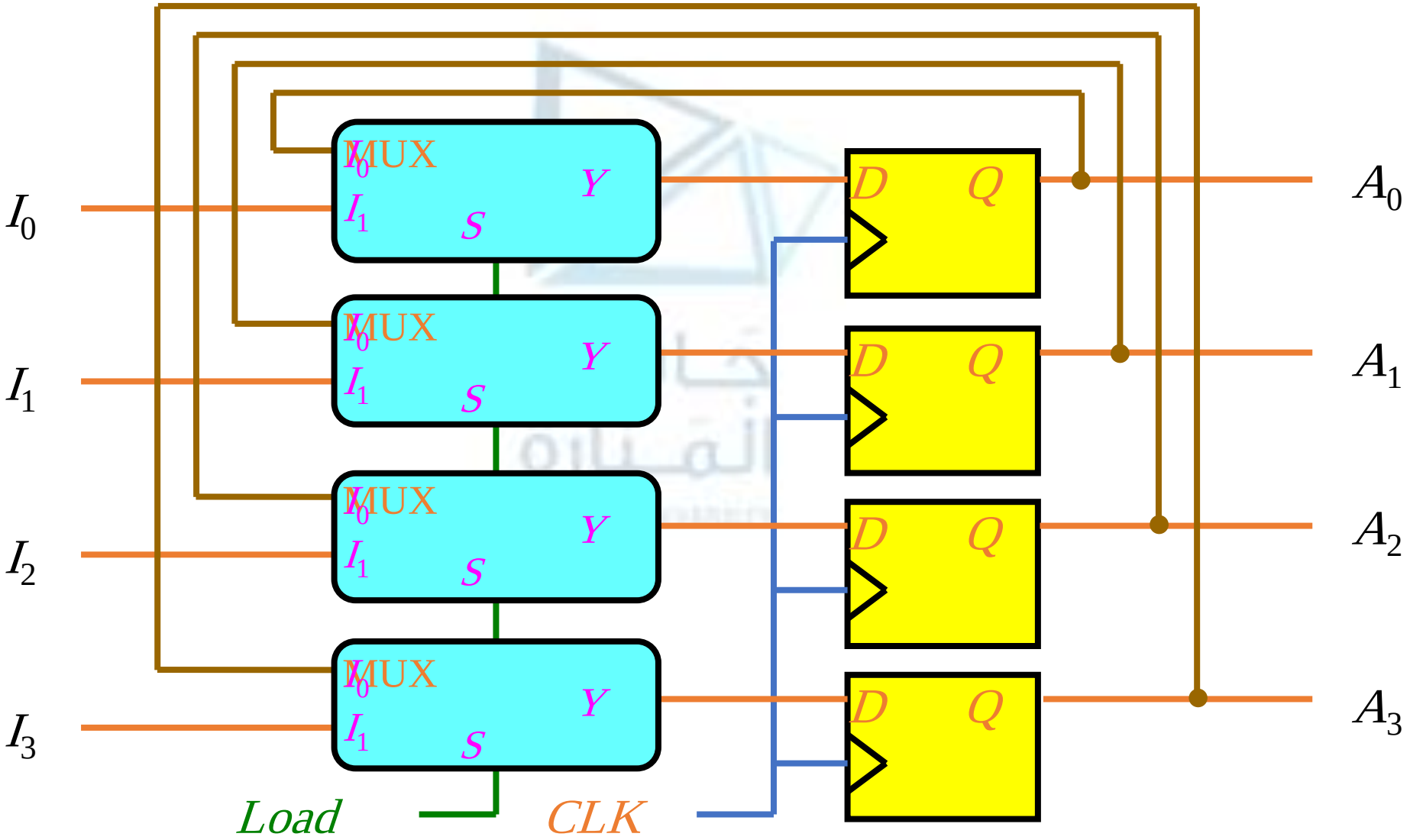
- Should we block the “Clock” to keep the “Data”?





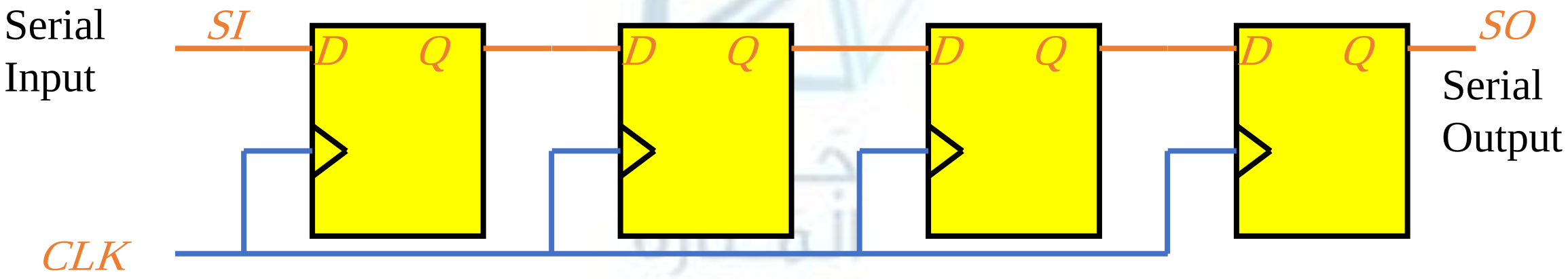
Registers with Parallel Load

- Circulate the “old data”

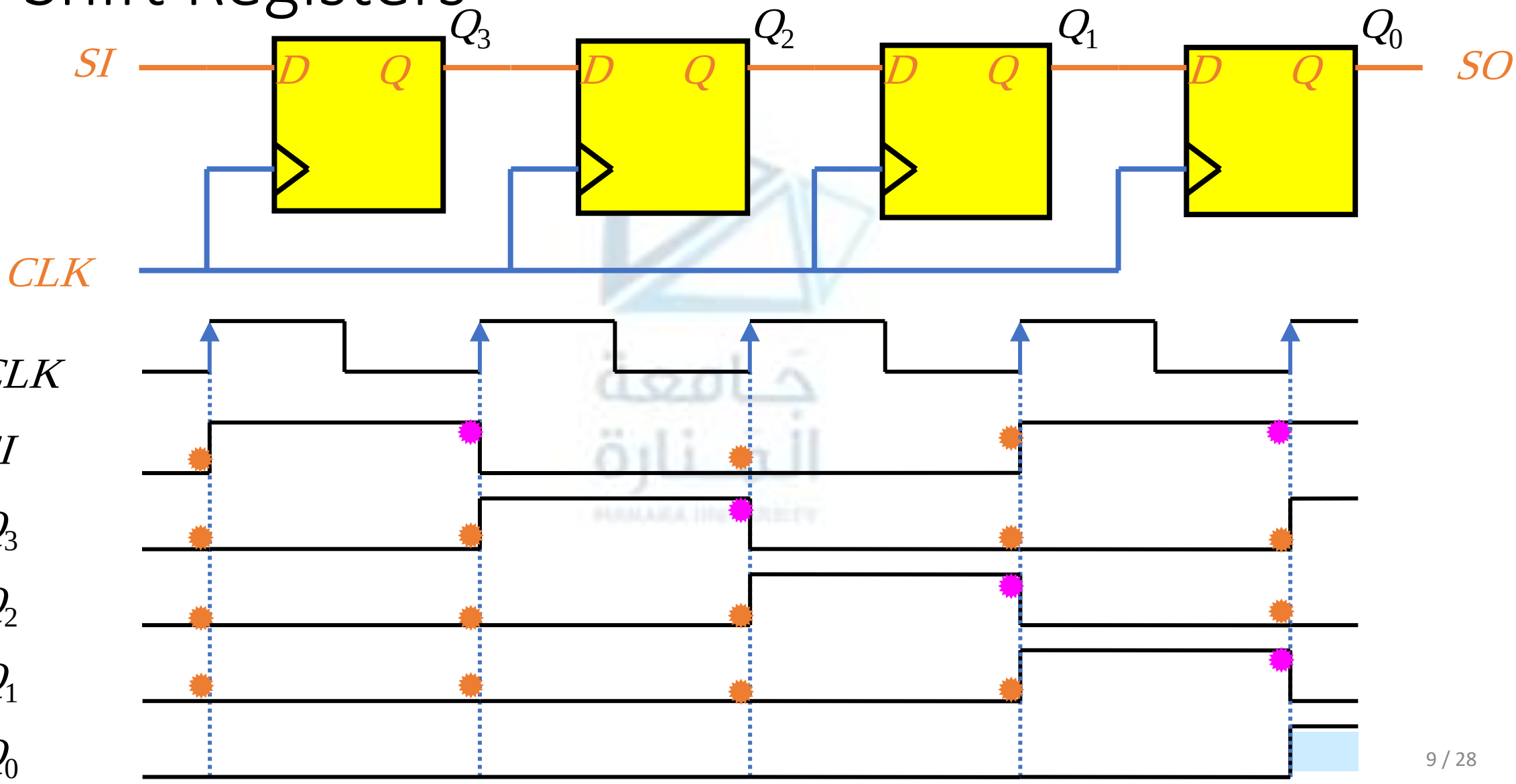


Shift Registers

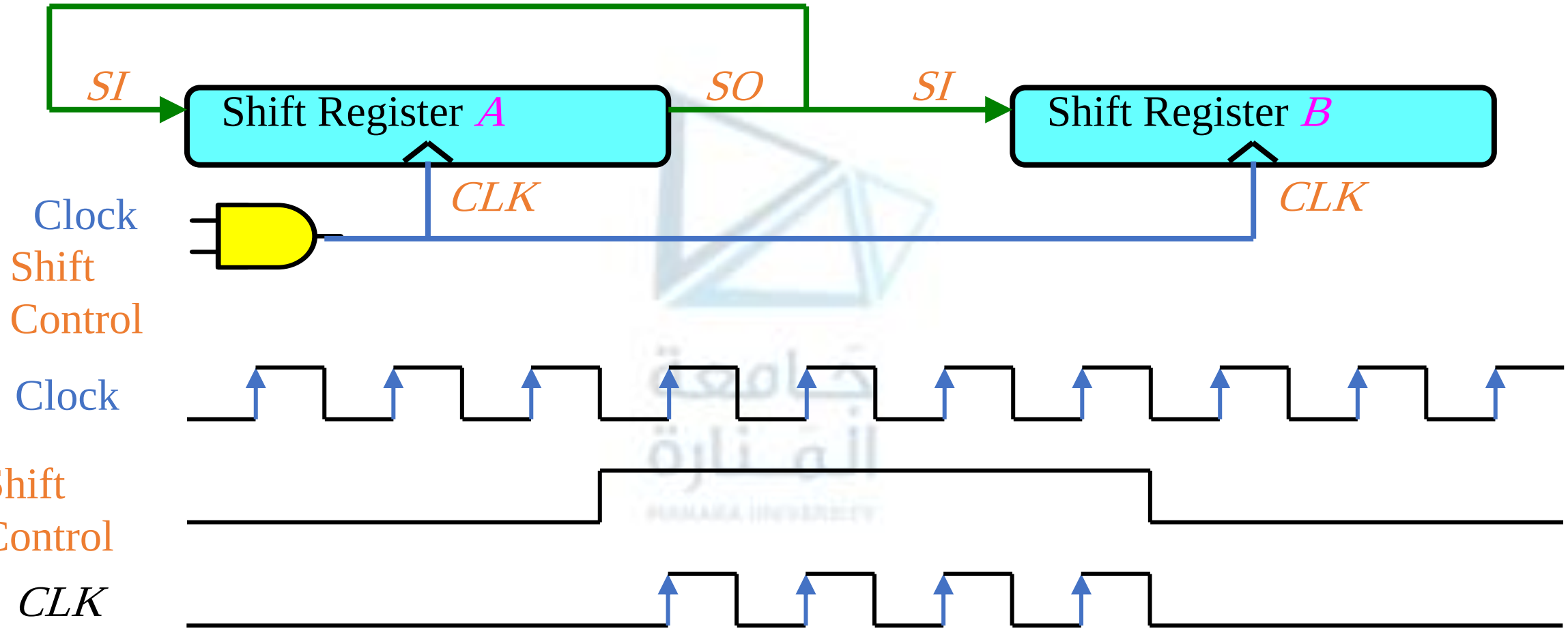
- 4-Bit Shift Register



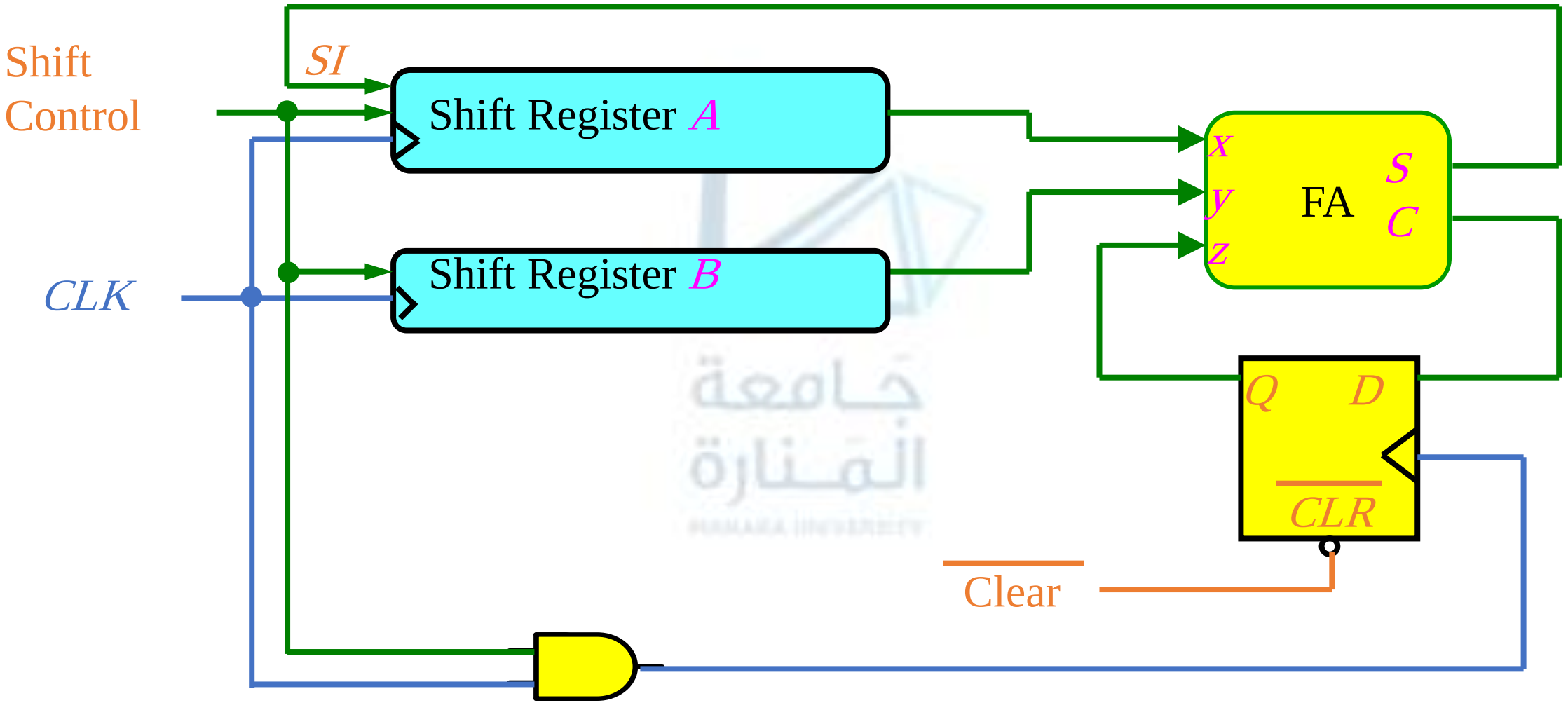
Shift Registers



Serial Transfer

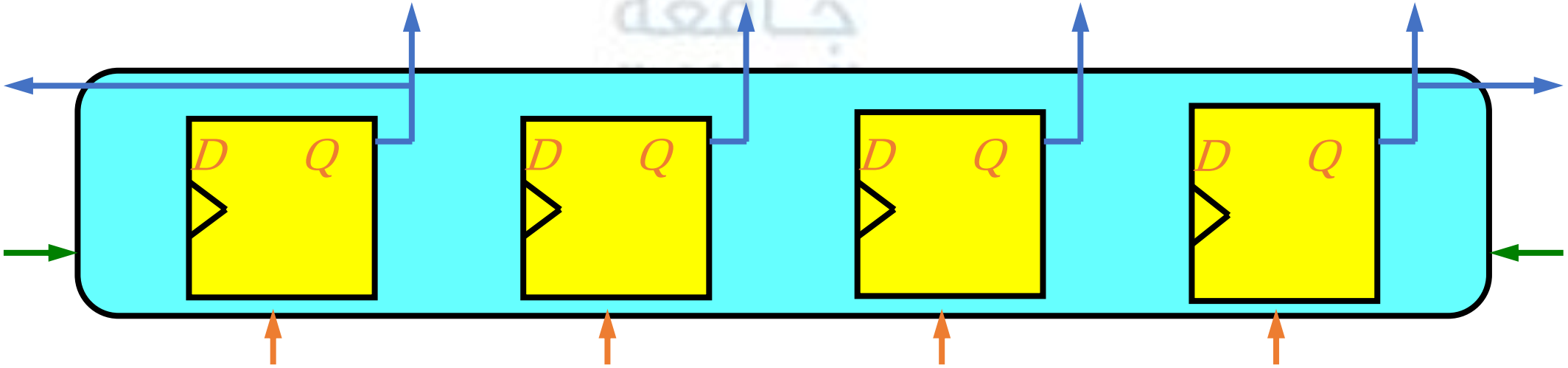


Serial Addition

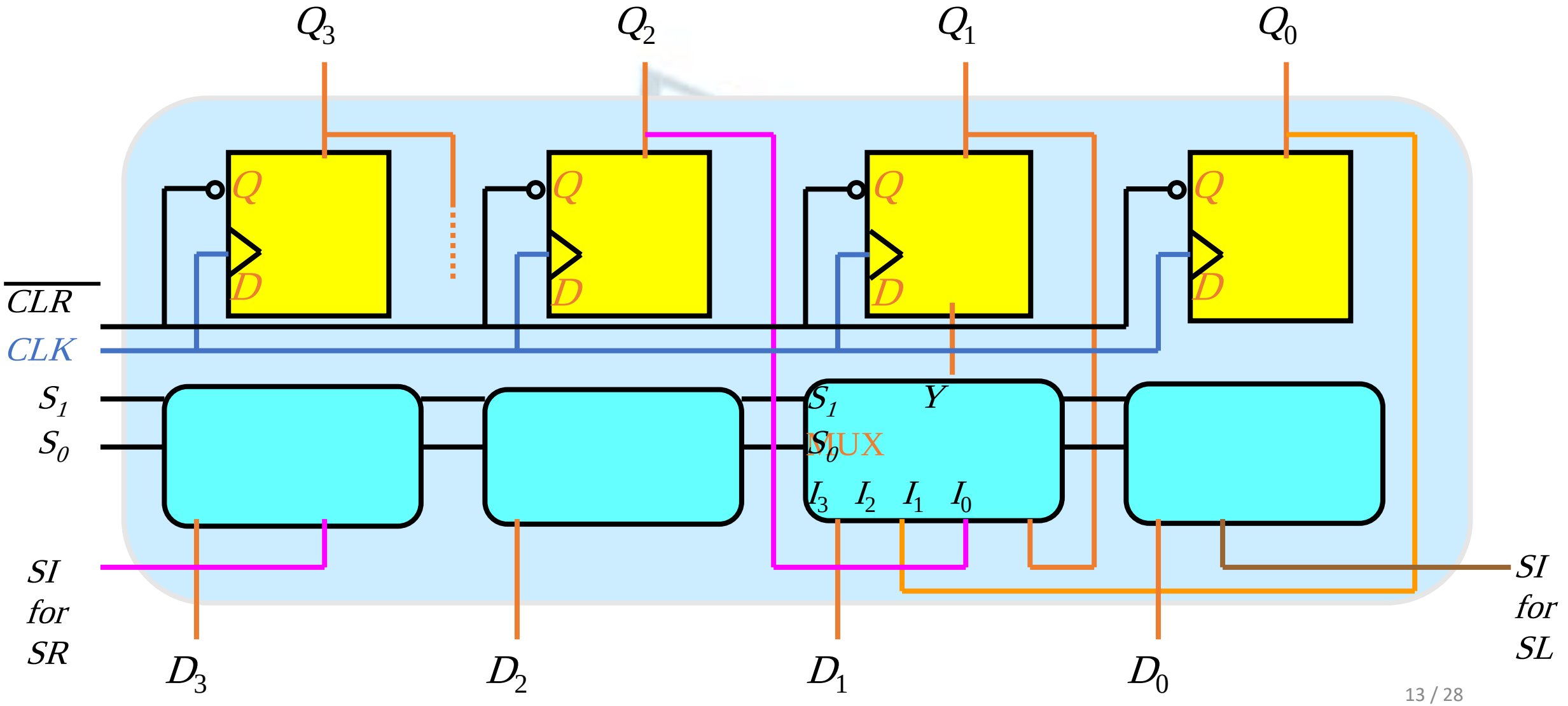


Universal Shift Register

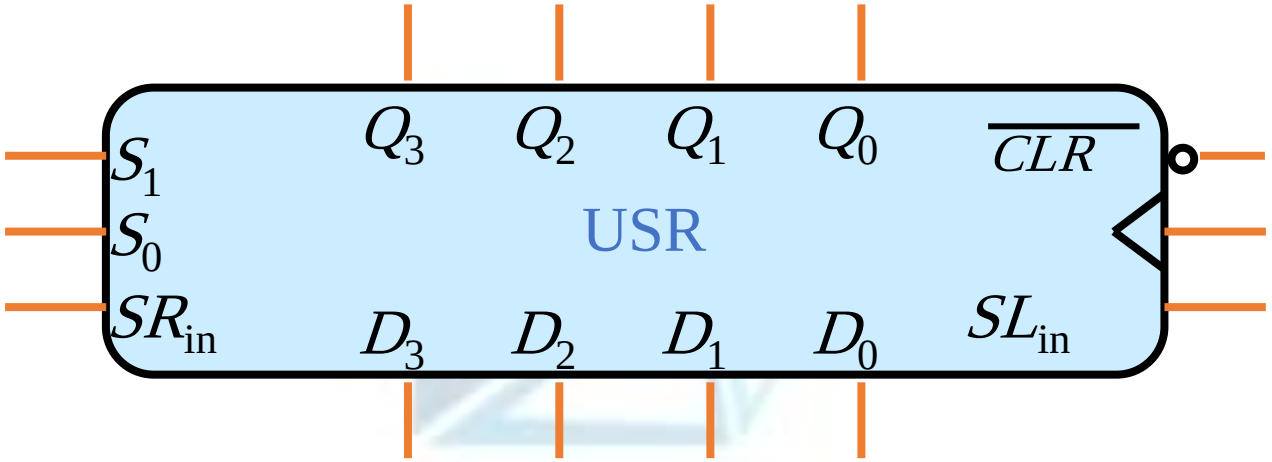
- Parallel-in Parallel-out
- Serial-in Serial-out
- Serial-in Parallel-out
- Parallel-in Serial-out



Universal Shift Register



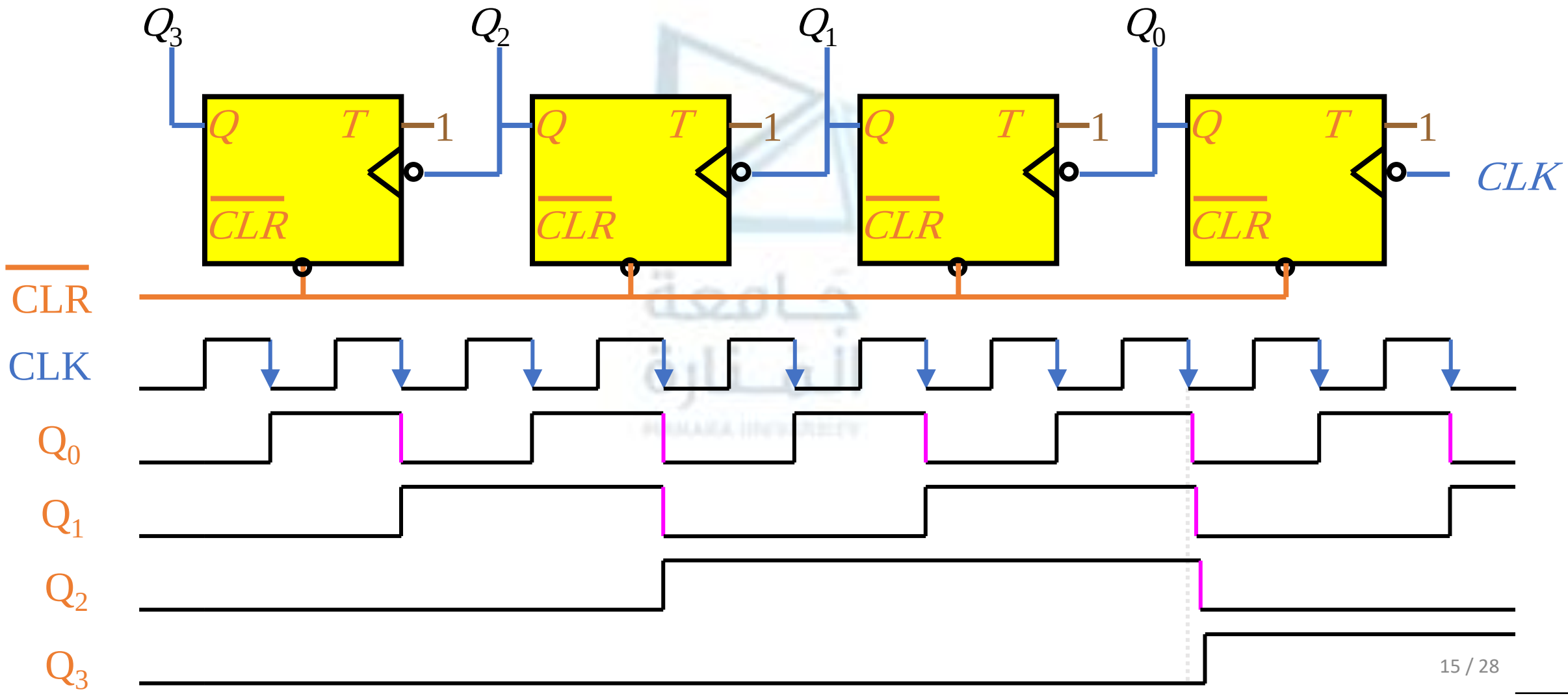
Universal Shift Register



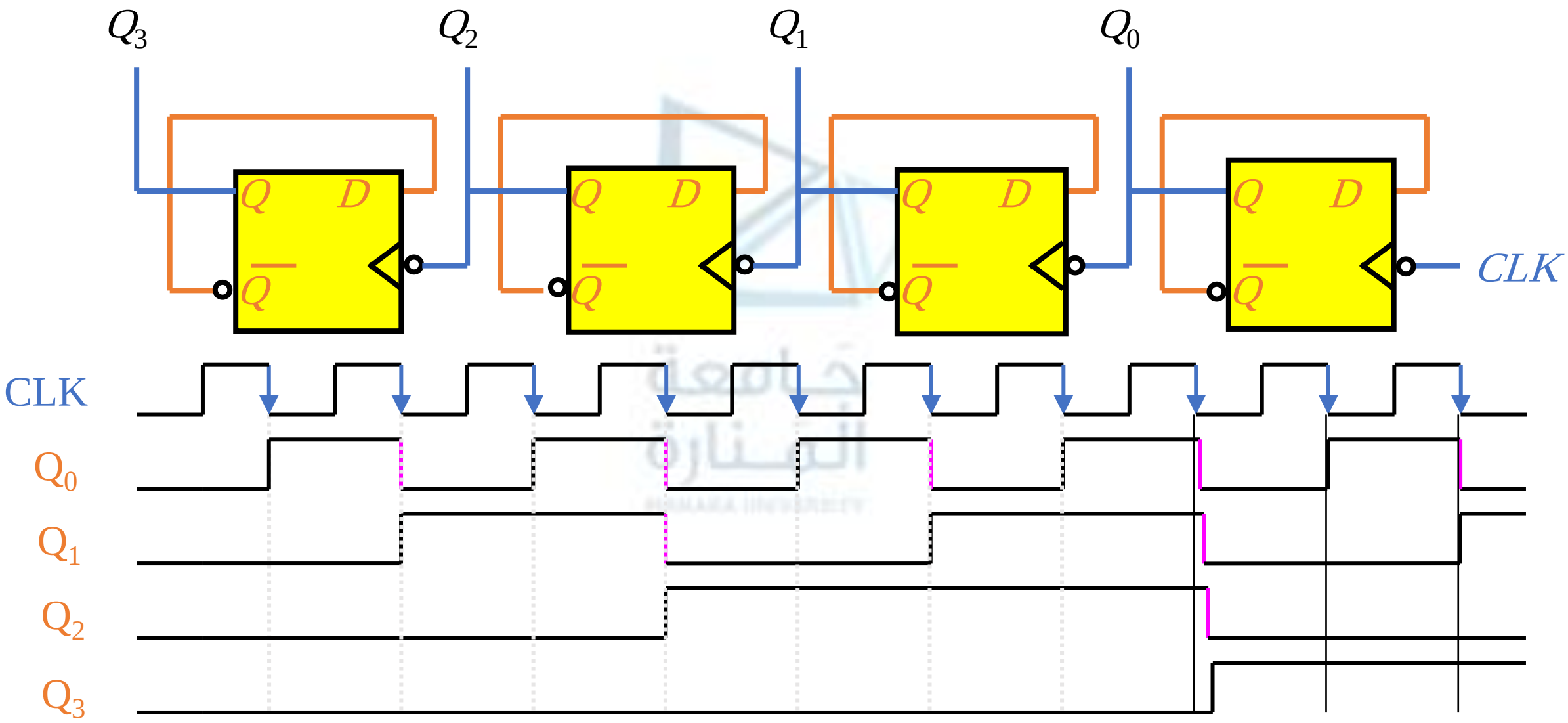
Mode Control		Register Operation
S_1	S_0	
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

Ripple Counters

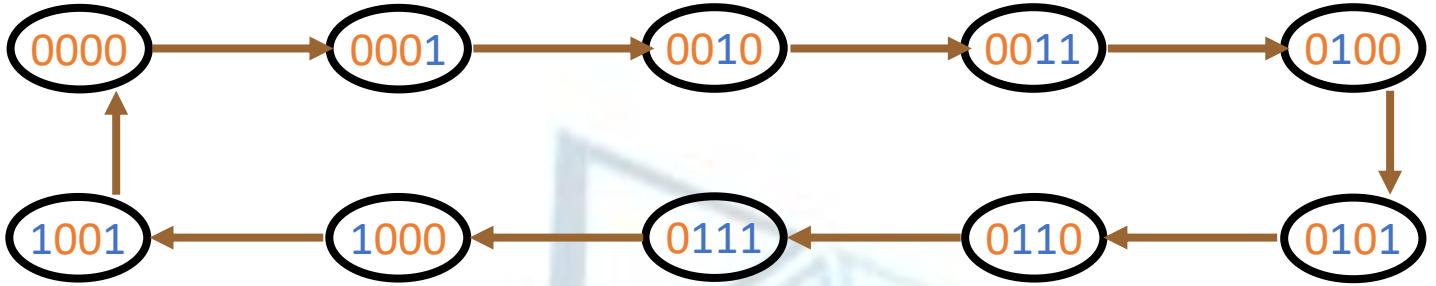
- Ripple ↔ Asynchronous

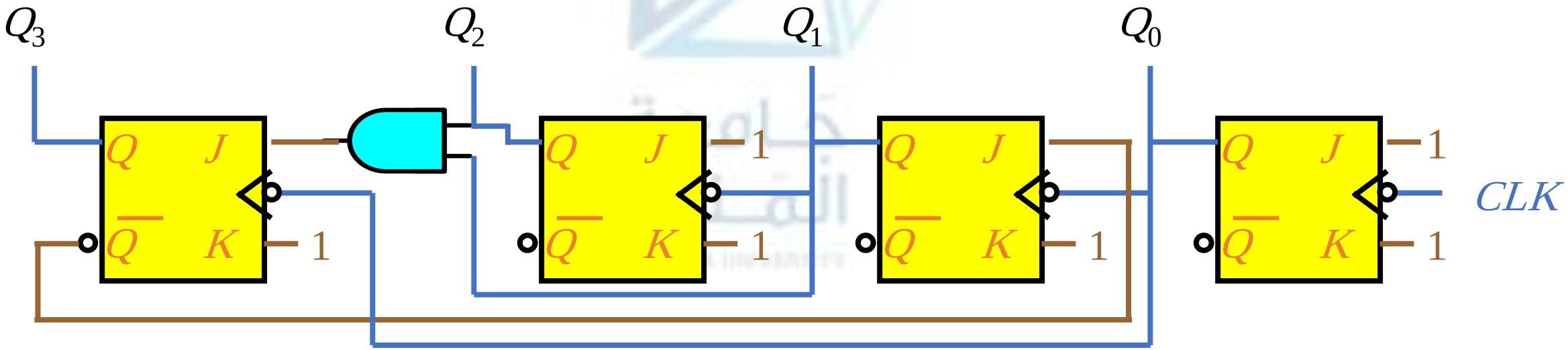


Ripple Counters

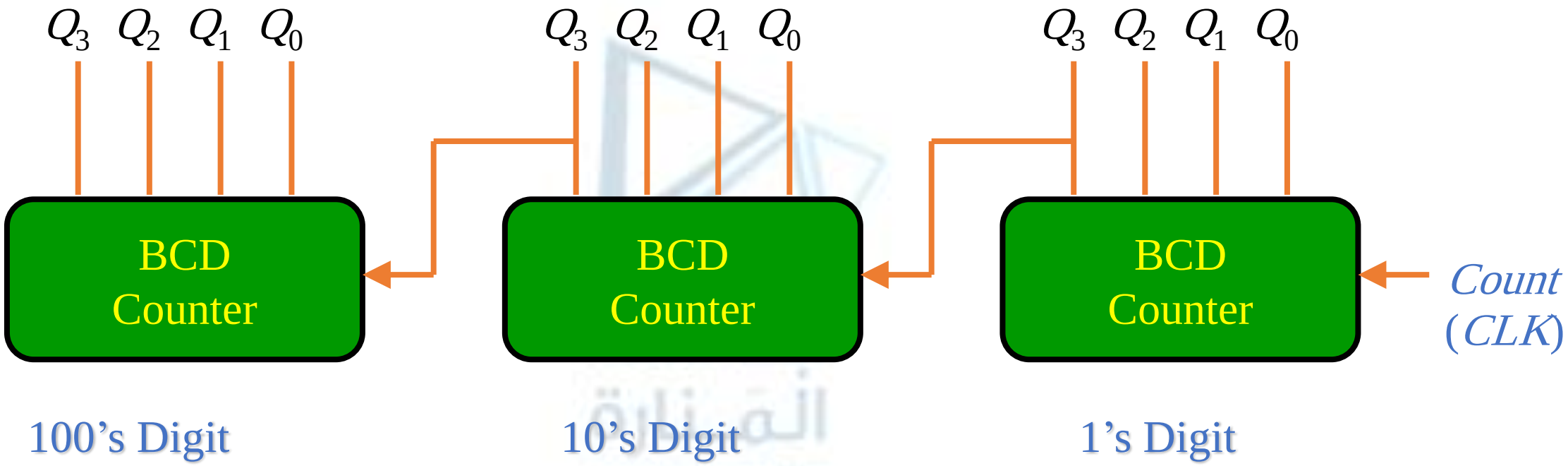


BCD Ripple Counter

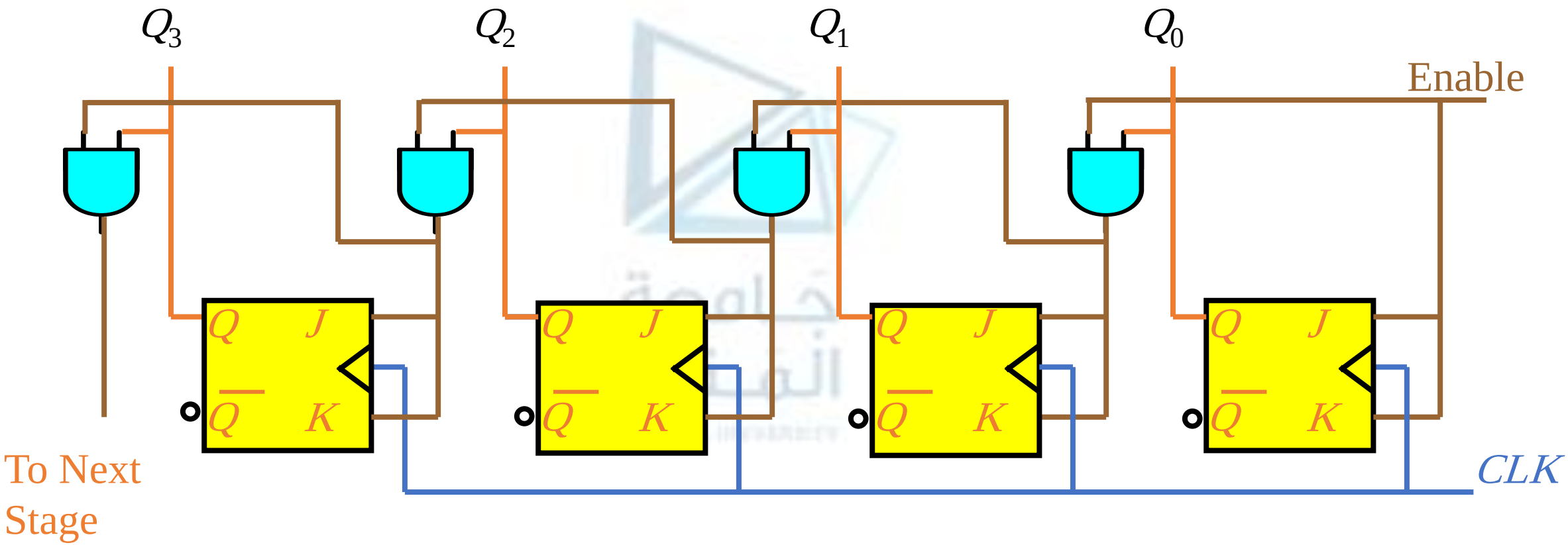




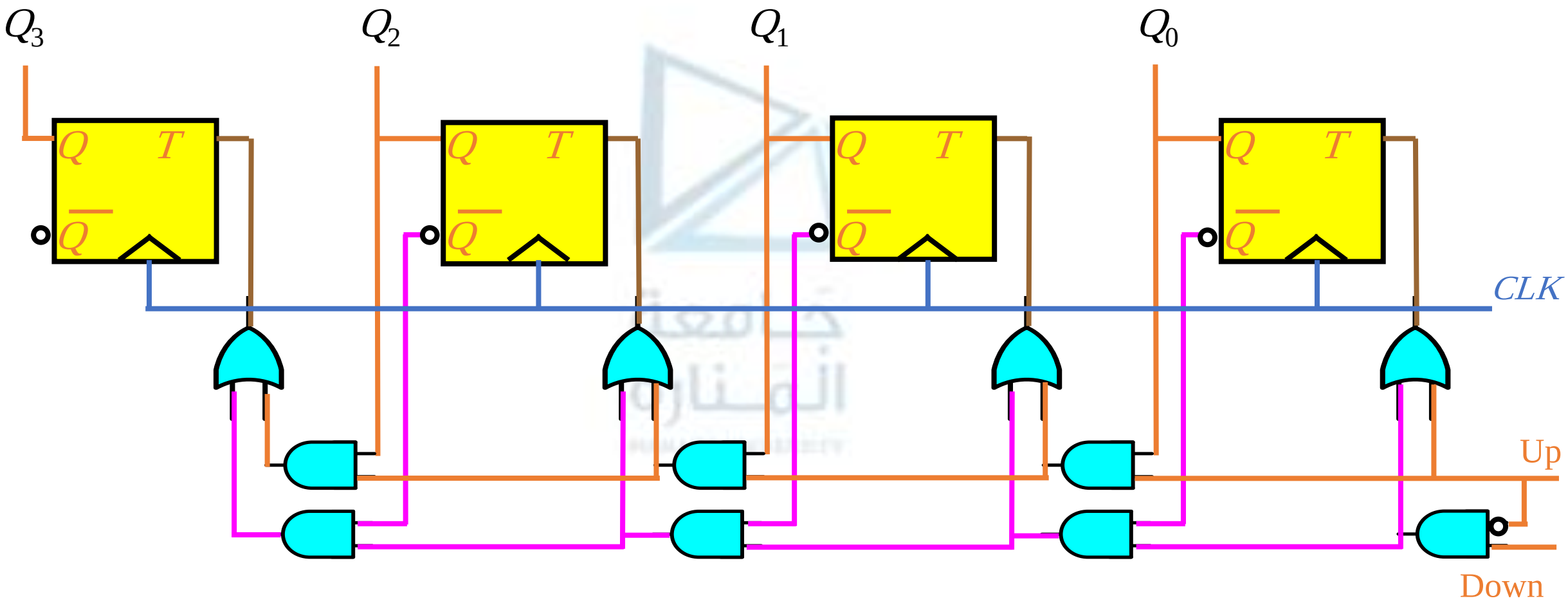
Decades Counter



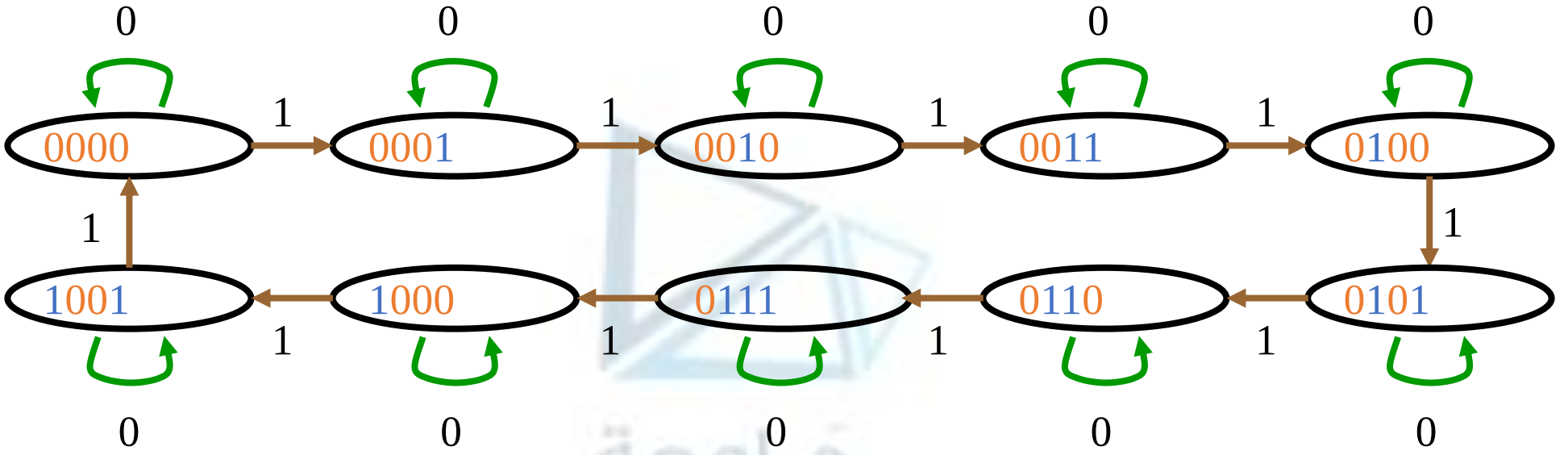
Synchronous Binary Counter

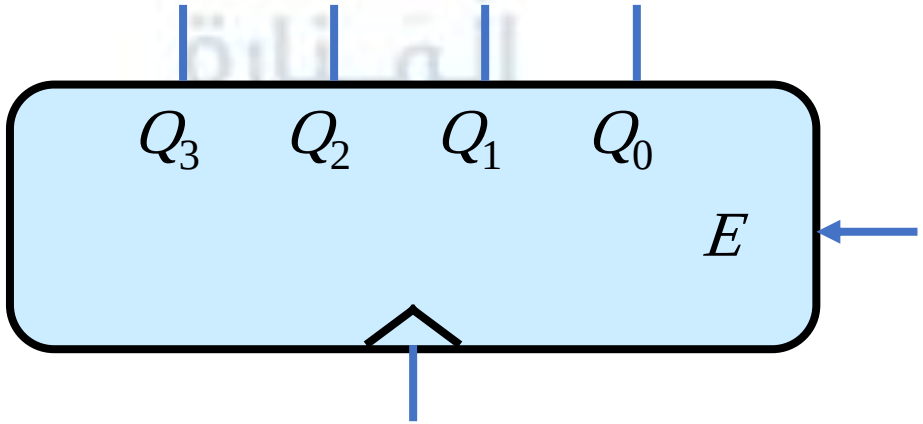


Up-Down Binary Counter

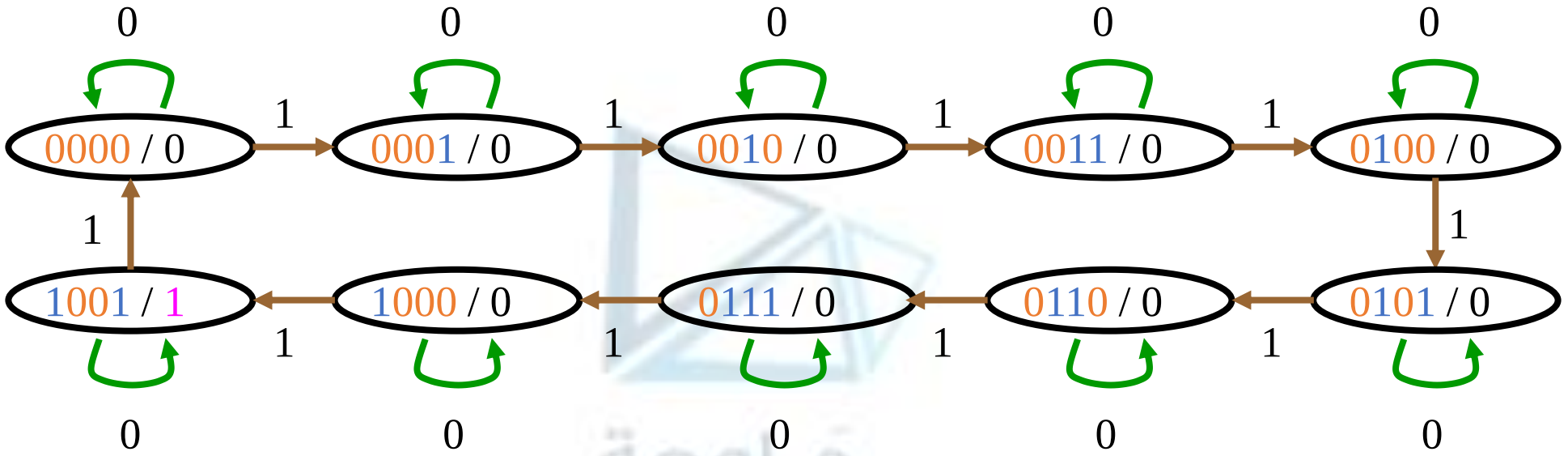


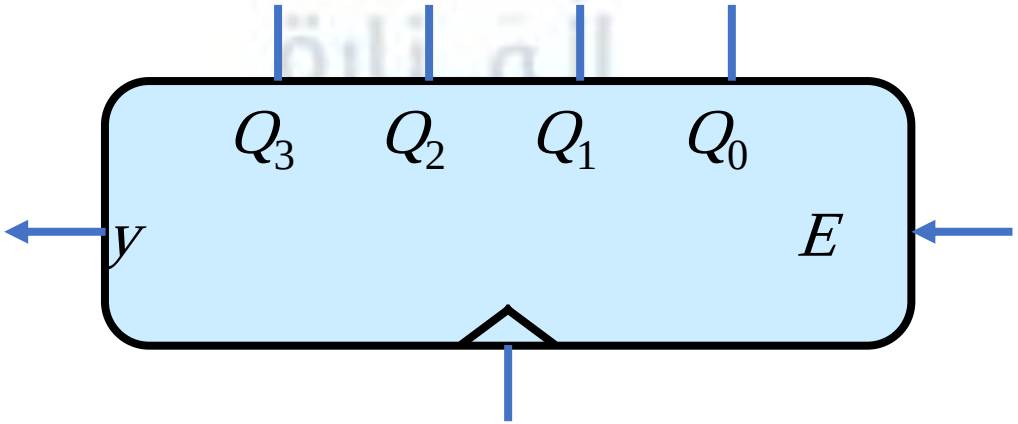
BCD Counter


0
0
0
0
0
1
1
1
1
0000
0001
0010
0011
0100
1
1
1001
1000
0111
0110
0101
1
1
1
1
0
0
0
0
0


Q_3
Q_2
Q_1
Q_0
E

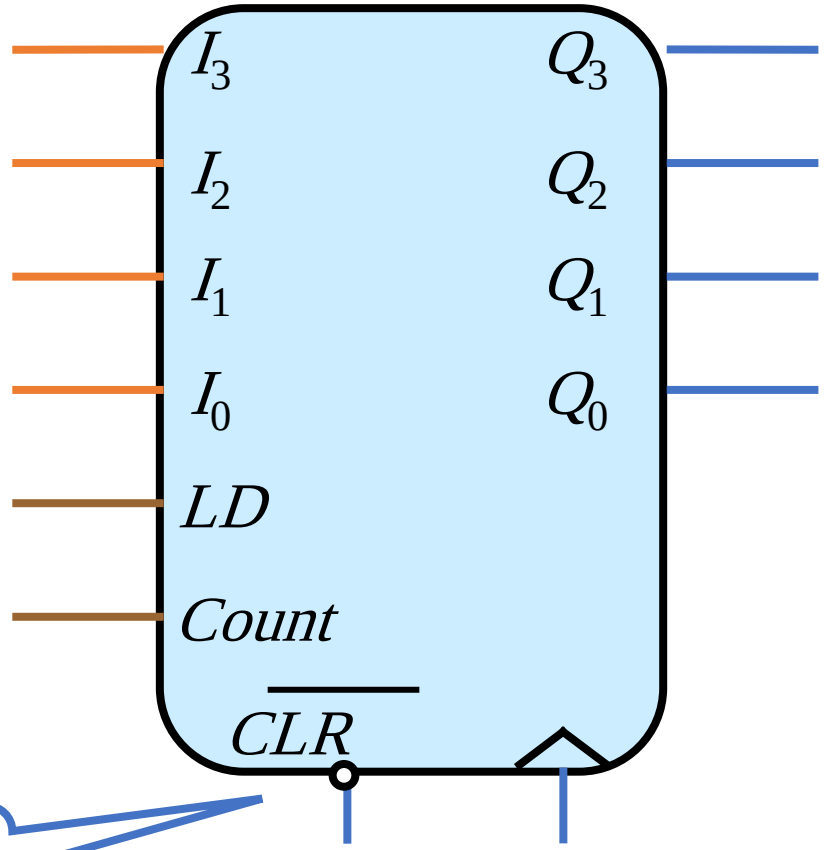
BCD Counter


0
0
0
0
0
1
1
1
1
0000 / 0
0001 / 0
0010 / 0
0011 / 0
0100 / 0
1
1
1001 / 1
1000 / 0
0111 / 0
0110 / 0
0101 / 0
1
1
1
1
0
0
0
0
0


Q_3
Q_2
Q_1
Q_0
y
E

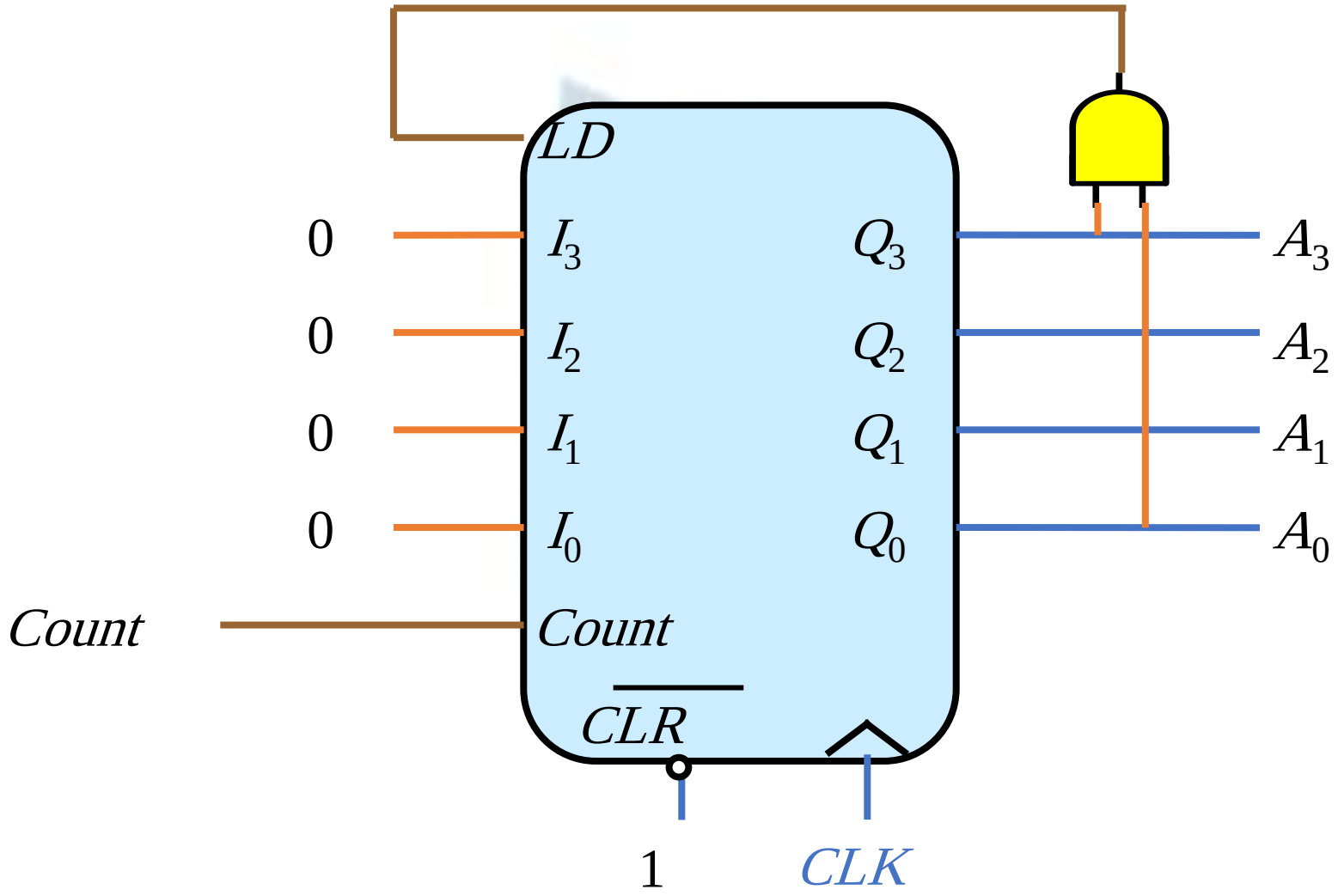
Binary Counter with Parallel Load

$\overline{CLR}$	LD	Count	Q(t+1)
0	x	x	0
1	0	0	Q(t)
1	0	1	Q(t)+1
1	1	x	I

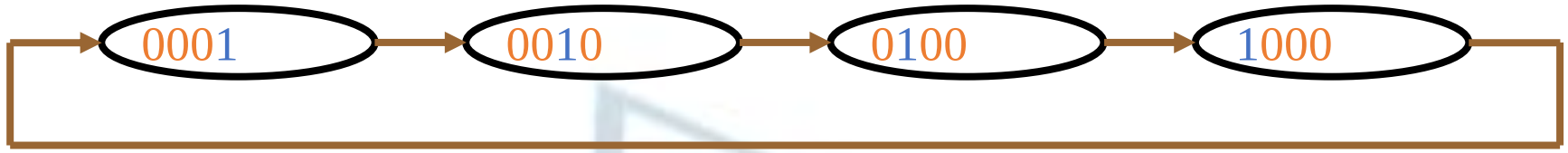


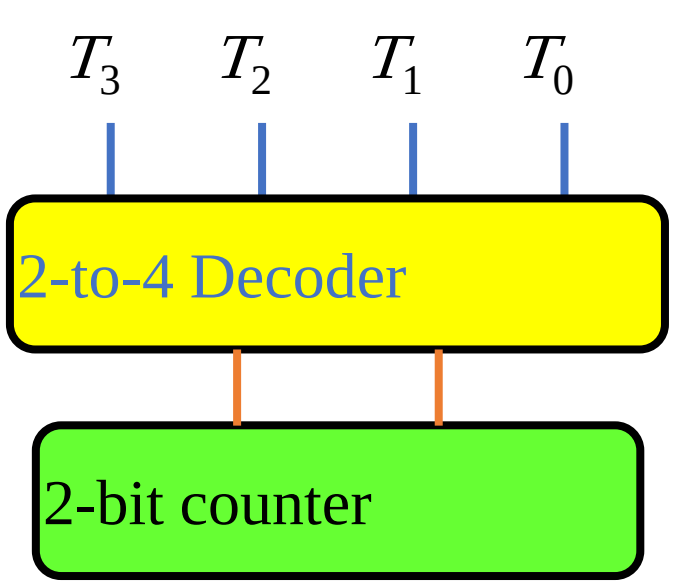
Usually Asynchronous Clear

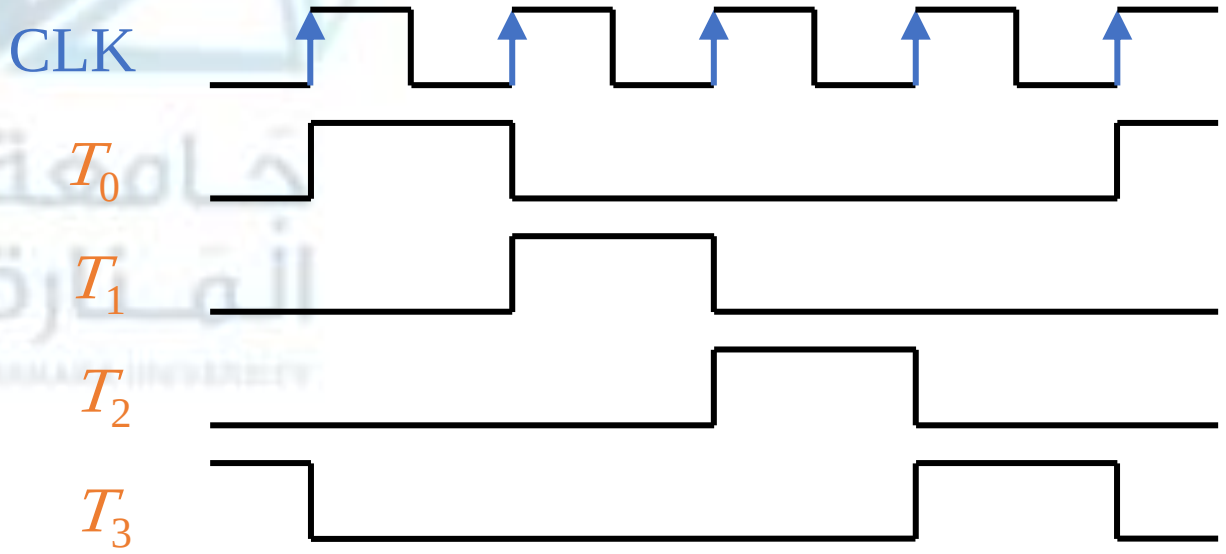
BCD Counter Example



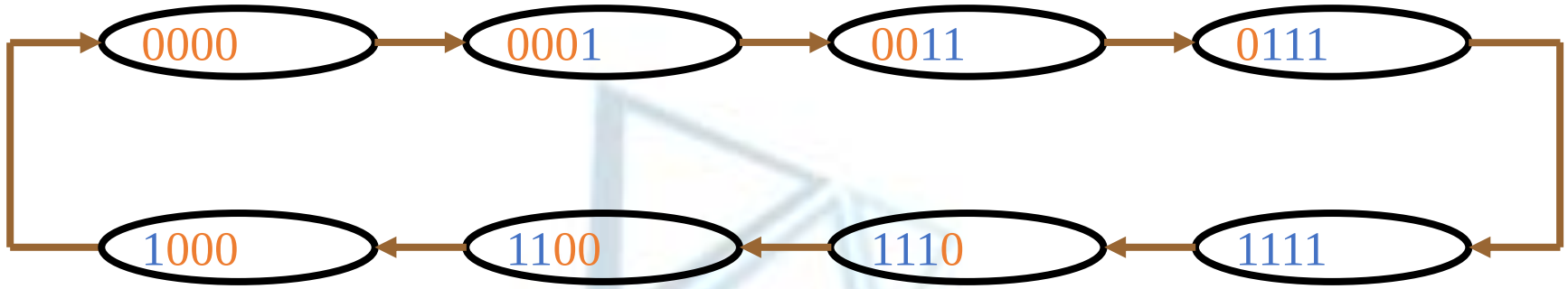
Ring Counter

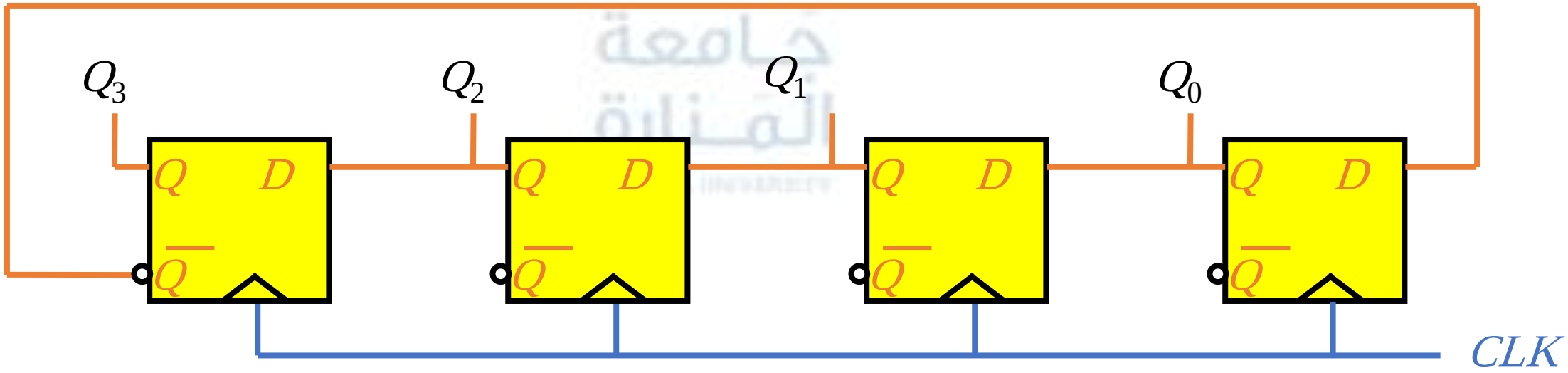






Johnson Counter





Homework

- Mano
  - Chapter 6
    - 6-2
    - 6-3
    - 6-4
    - 6-13
    - 6-14
    - 6-16
    - 6-18

Homework

6-2 **Include a synchronous clear input to the "Register with Parallel Load". The modified register will have a parallel load capability and a synchronous clear capability. The register is cleared synchronously when the clock goes through a positive transition and the clear input is equal to 1.**

6-3 **What is the difference between serial and parallel transfer? Explain how to convert serial data to parallel and parallel data to serial. What type of register is needed?**

Homework

6-4 **The content of a 4-bit register is initially 1101. The register is shifted six times to the right with the serial input being 101101. What is the content of the register after each shift?**

6-13 **Show that a BCD ripple counter can be constructed using a 4-bit binary ripple counter with asynchronous clear and a NAND gate that detects the occurrence of count 1010.**

6-14 **How many flip-flop will be complemented in a 10-bit binary ripple counter to reach the next count after the following count:**

(a) 1001100111

(b) 0011111111

(c) 1111111111

Homework

6-16 **The BCD ripple counter has four flip-flops and 16 states, of which only 10 are used. Analyze the circuit and determine the next state for each of the other six unused states. What will happen if a noise signal sends the circuit to one of the unused states?**

6-18 **What operation is performed in the up-down counter when both the up and down inputs are enabled? Modify the circuit so that when both inputs are equal to 1, the counter does not change state, but remains in the same count.**