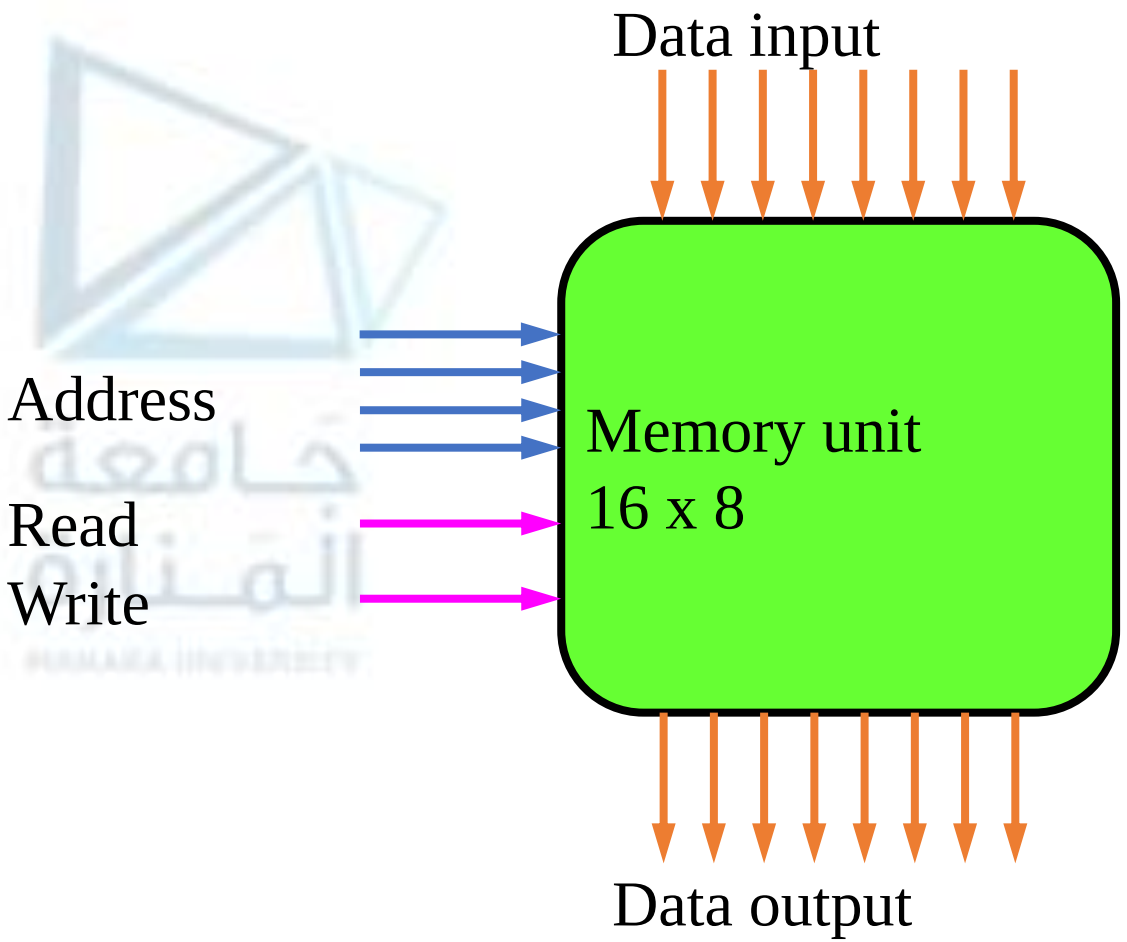
جامعة
المنارة
MANARA UNIVERSITY

Random-Access Memory (RAM)

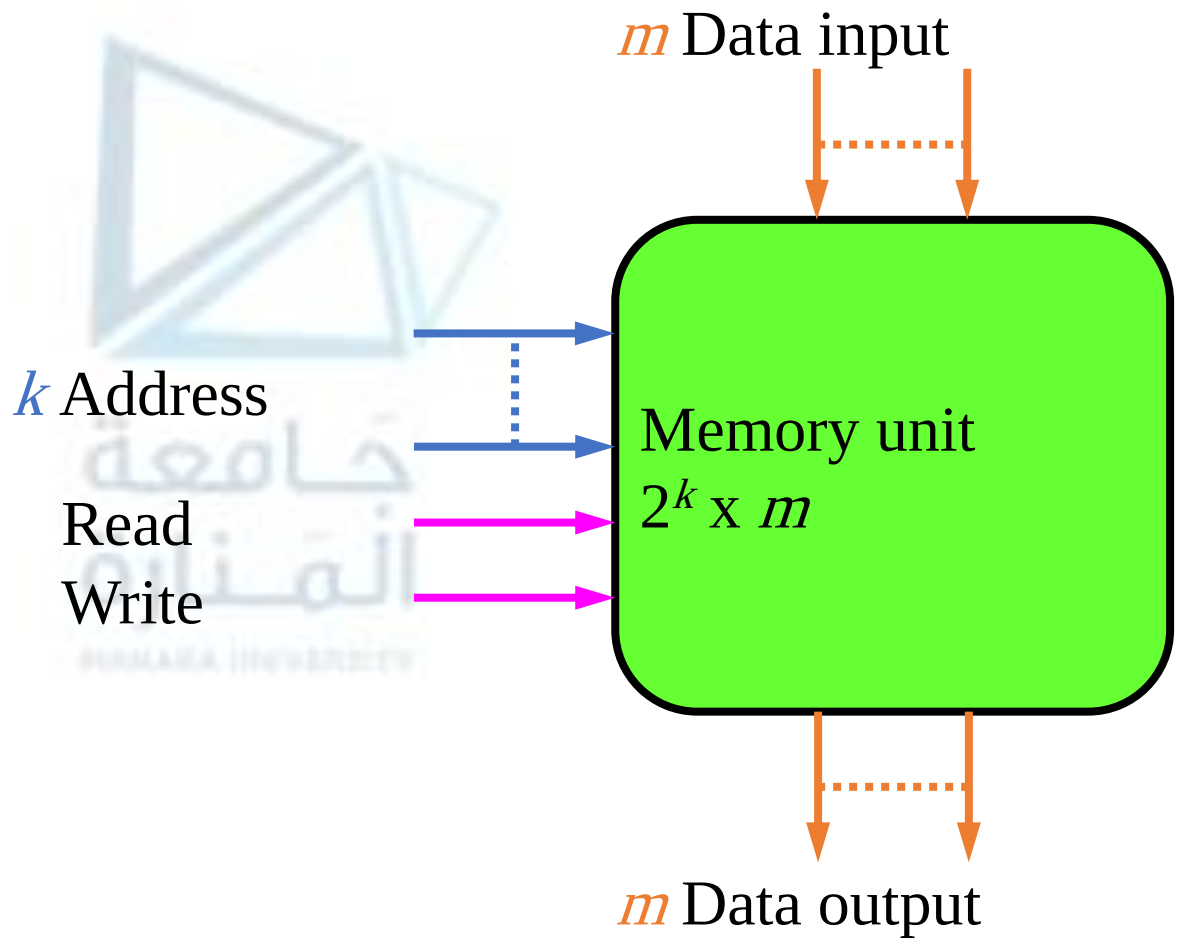
- Data Storage (Volatile)
- Locations (Address)
- Byte or Word



Random-Access Memory (RAM)

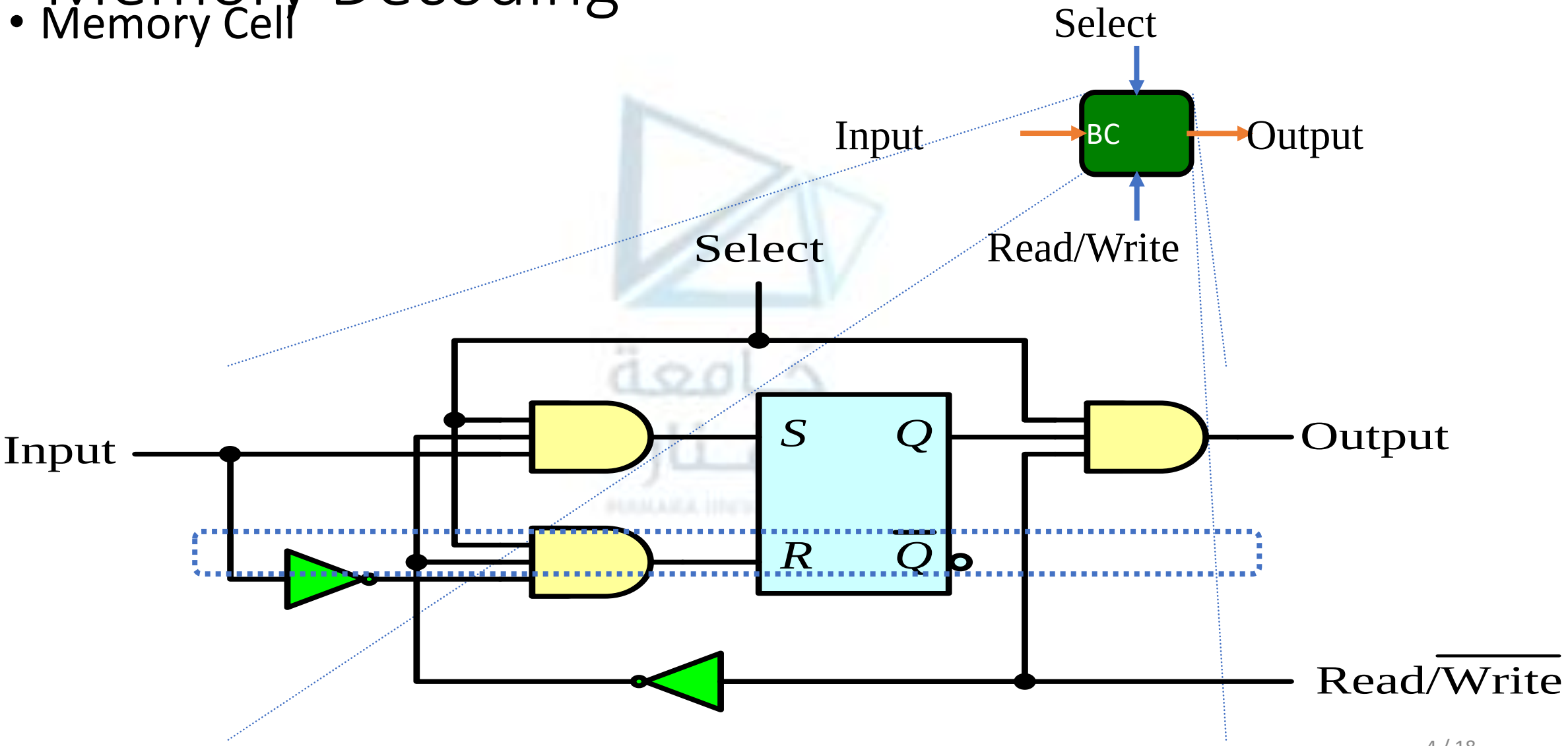
- Data Storage (Volatile)
- Locations (Address)
- Byte or Word

10 Address lines
➔ 1024 locations
= 1 K



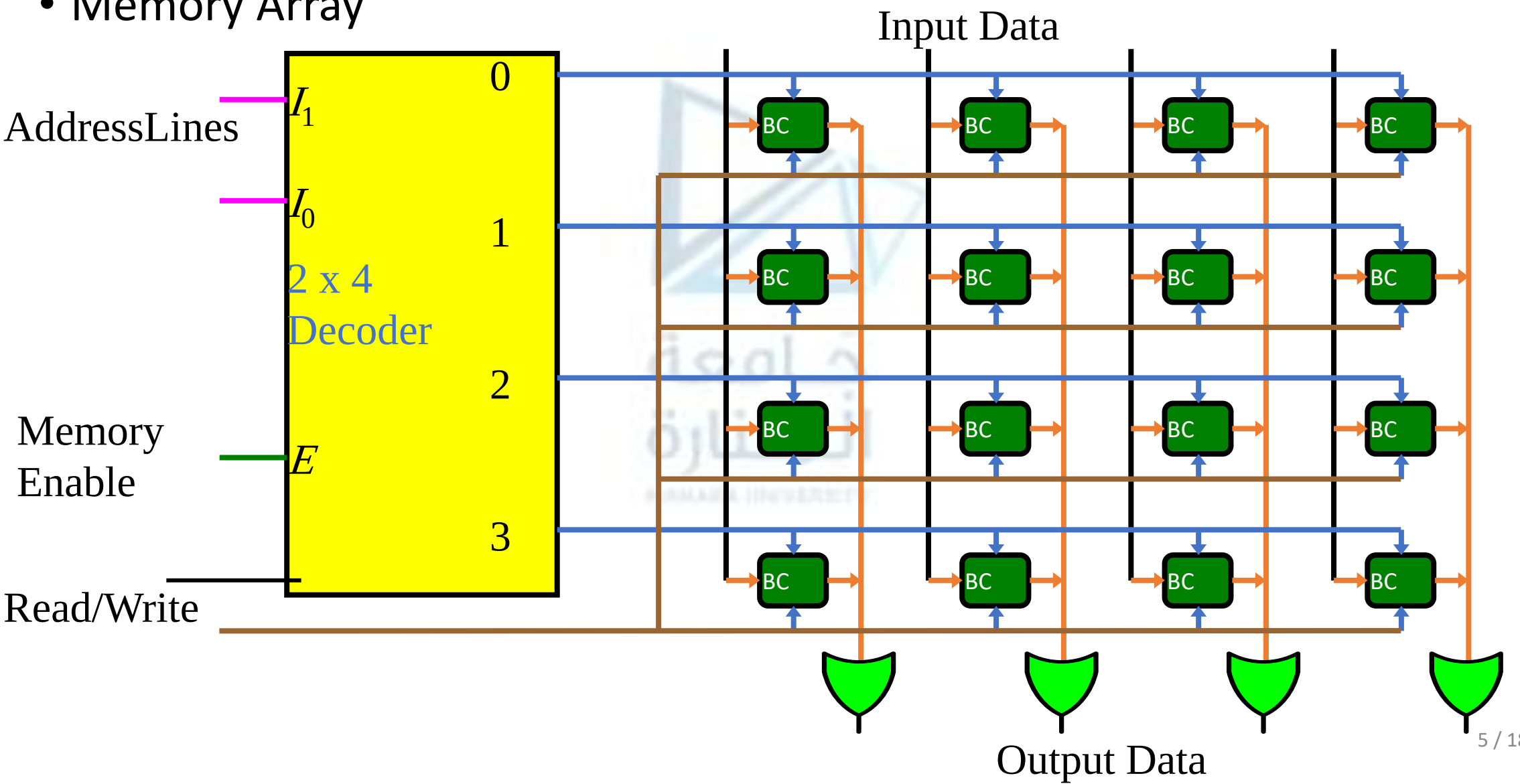
Memory Decoding

- Memory Cell

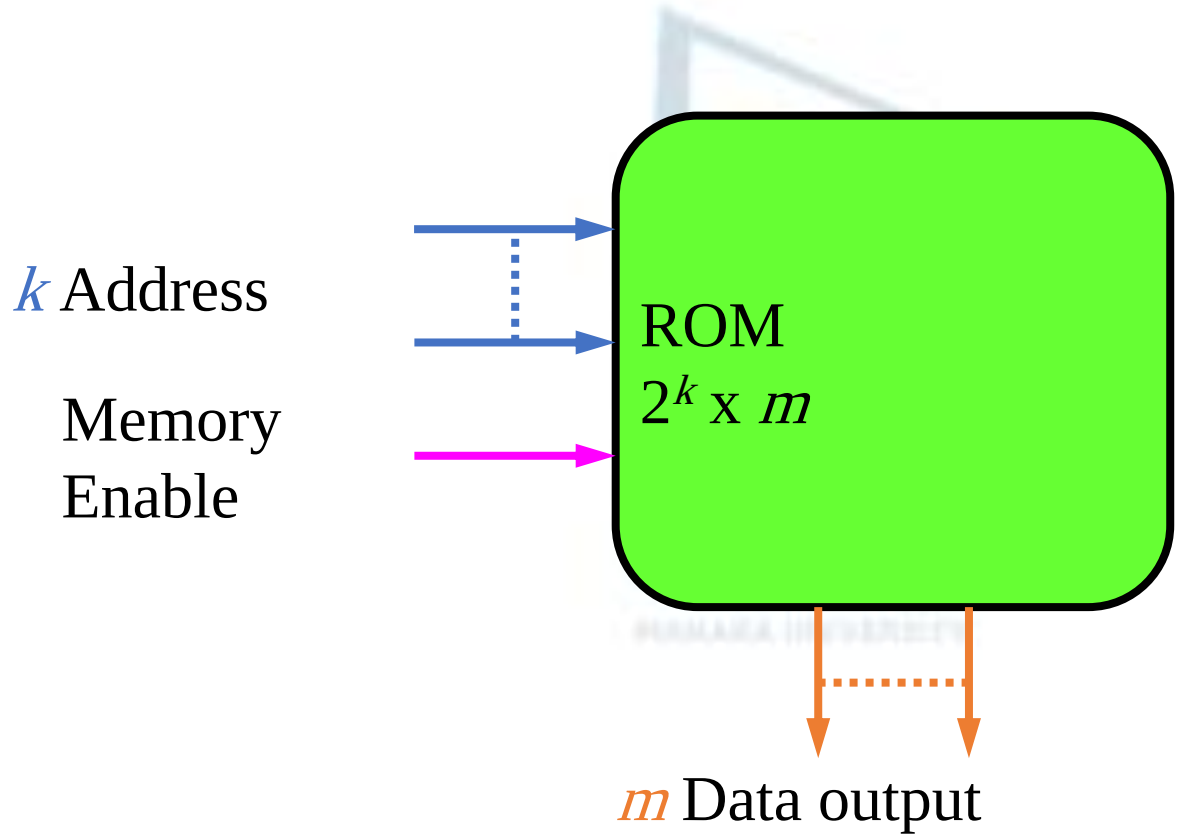


Memory Decoding

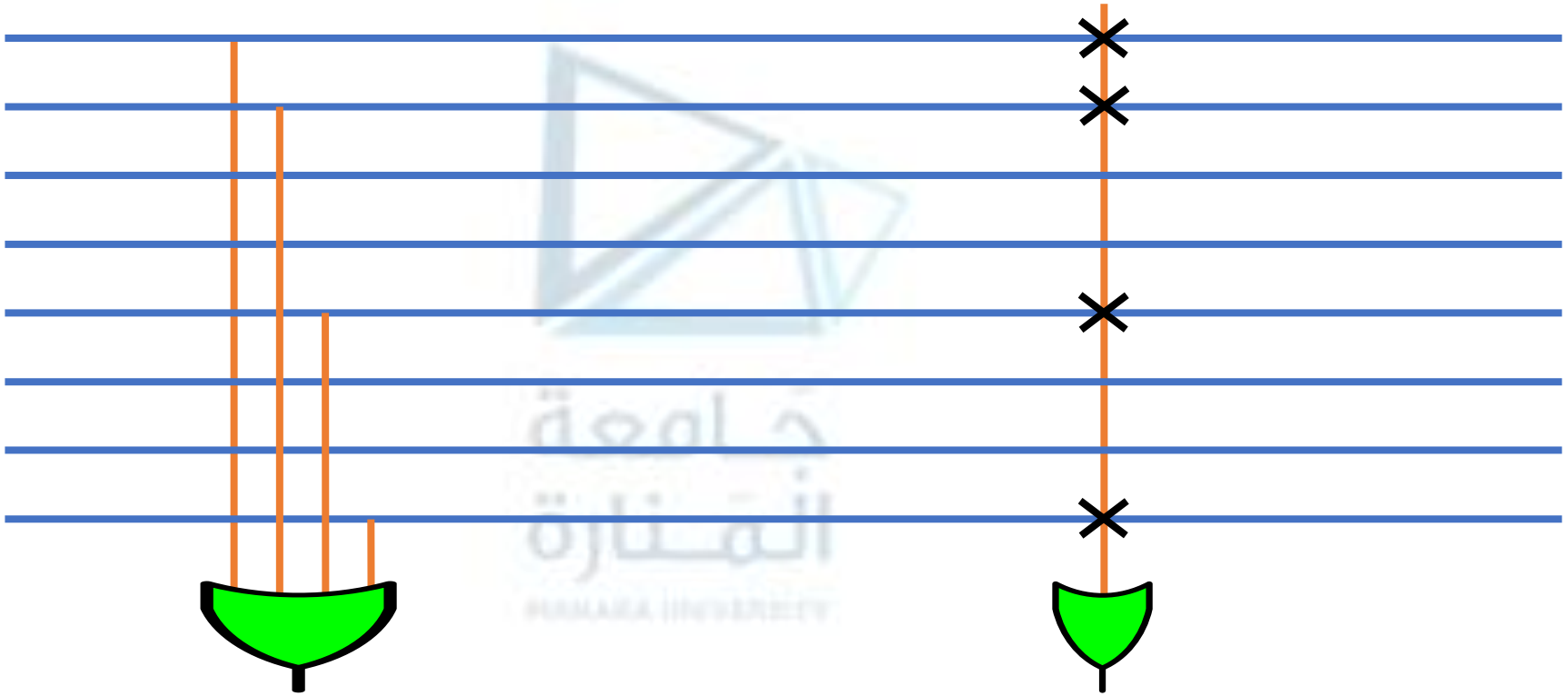
- Memory Array



Read-Only Memory (ROM)



Read-Only Memory (ROM)

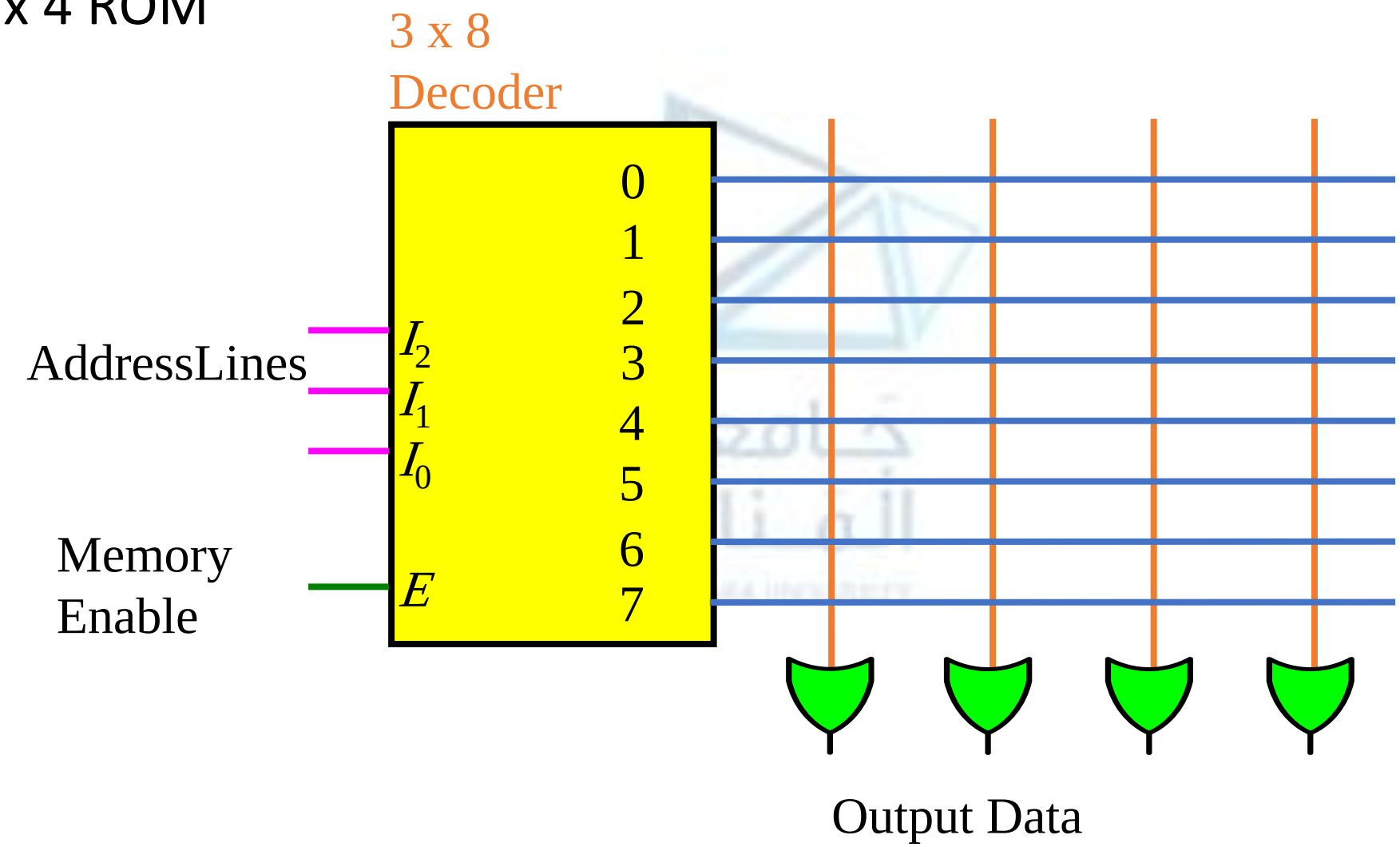


Conventional Symbol

Array Logic Symbol

Read-Only Memory (ROM)

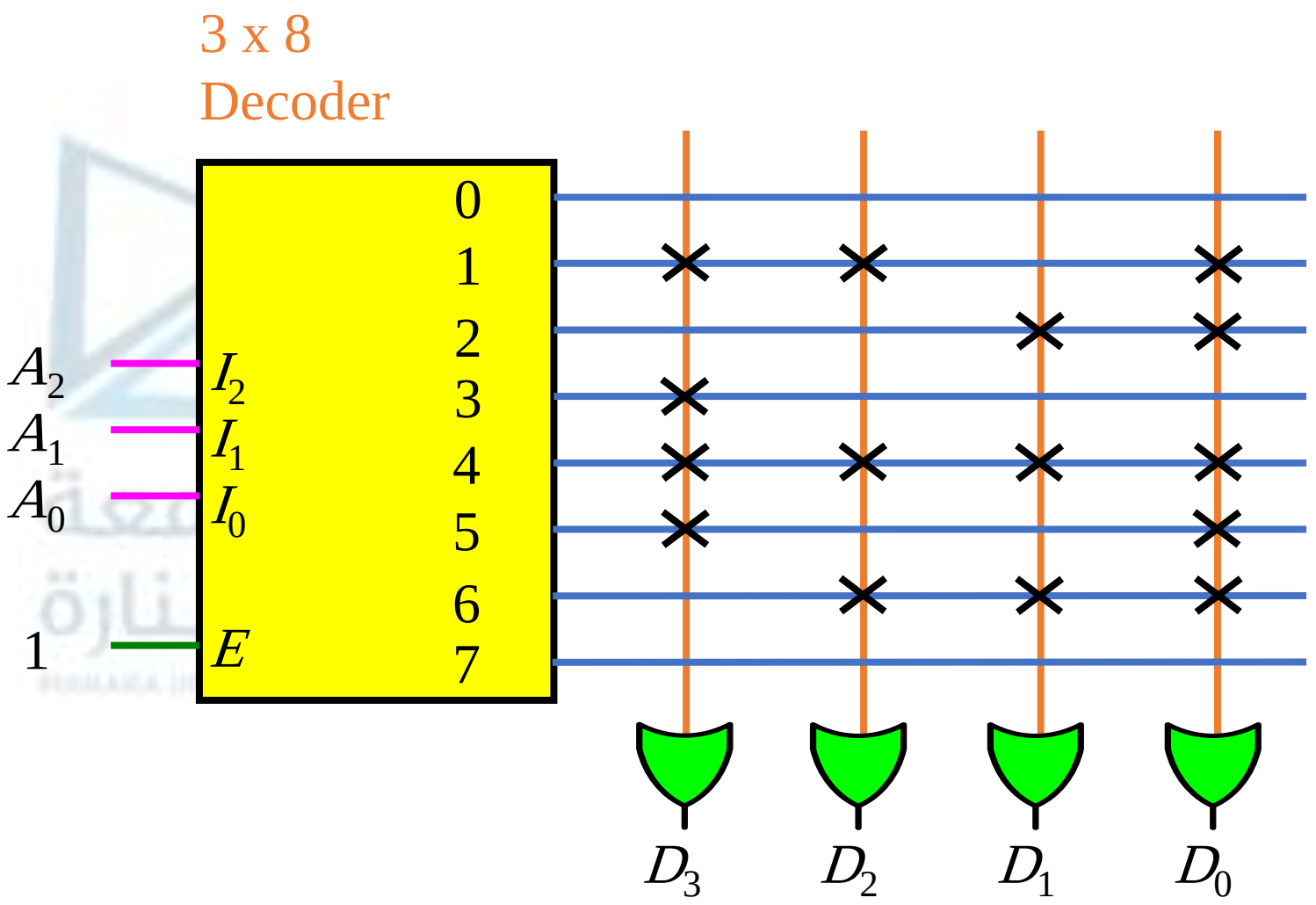
- 8 x 4 ROM



Read-Only Memory (ROM)

- 8 x 4 ROM

Address	Data
0 0 0	0 0 0 0
0 0 1	1 1 0 1
0 1 0	0 0 1 1
0 1 1	1 0 0 0
1 0 0	1 1 1 1
1 0 1	1 0 0 1
1 1 0	0 1 1 1
1 1 1	0 0 0 0

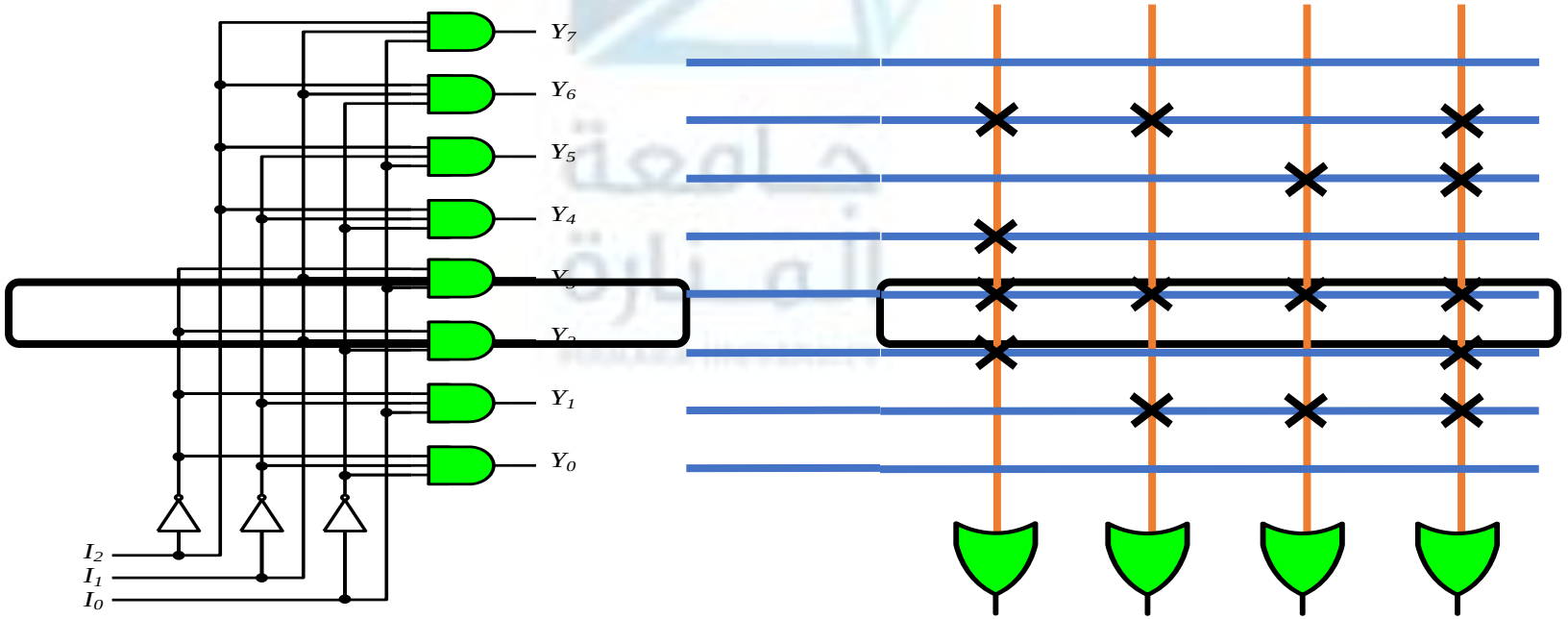


Types of ROMs

- Mask Programmed ROM
  - Programmed during manufacturing
- Programmable Read-Only Memory (PROM)
  - Blow out fuses to produce ‘0’
- Erasable Programmable ROM (EPROM)
  - Erase all data by *Ultra Violet* exposure
- Electrically Erasable PROM (EEPROM)
  - Erase the required data using an electrical signal

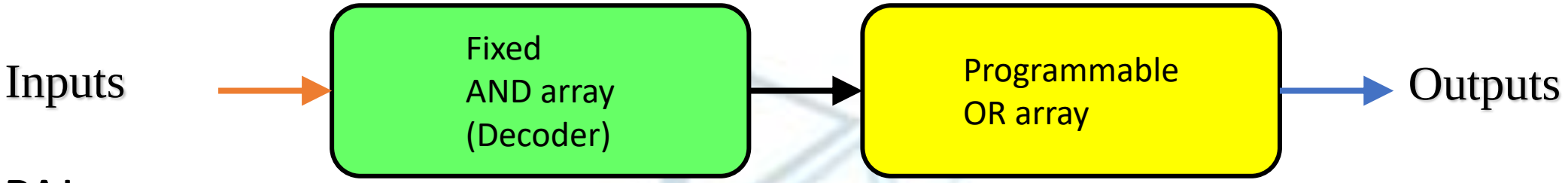
Programmable Logic Device (PLD)

- Boolean Functions:
  - Sums-of-Products
  - AND-plane followed by OR-plane

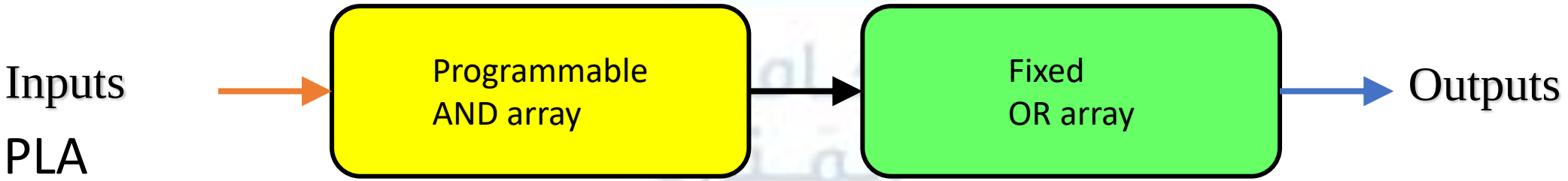


Programmable Logic Device (PLD)

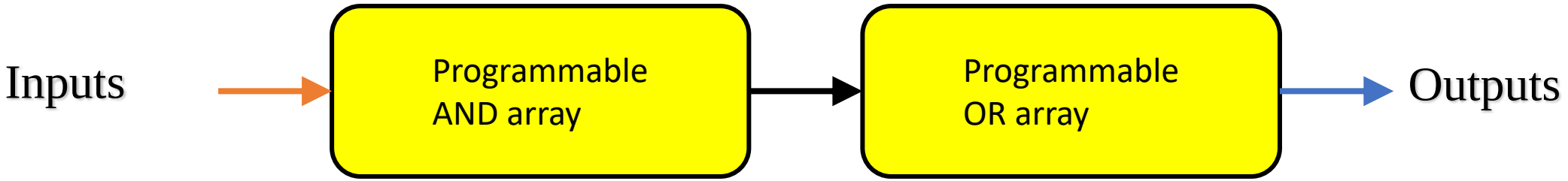
- PROM



- PAL



- PLA



Programmable Array Logic (PAL)

Example

$w(A,B,C,D) = \sum(2,12,13)$

$x(A,B,C,D) = \sum(7,8,9,10,11,12,13,14,15)$

$y(A,B,C,D) = \sum(0,2,3,4,5,6,7,8,10,11,15)$

$z(A,B,C,D) = \sum(1,2,8,12,13)$

Simplify:

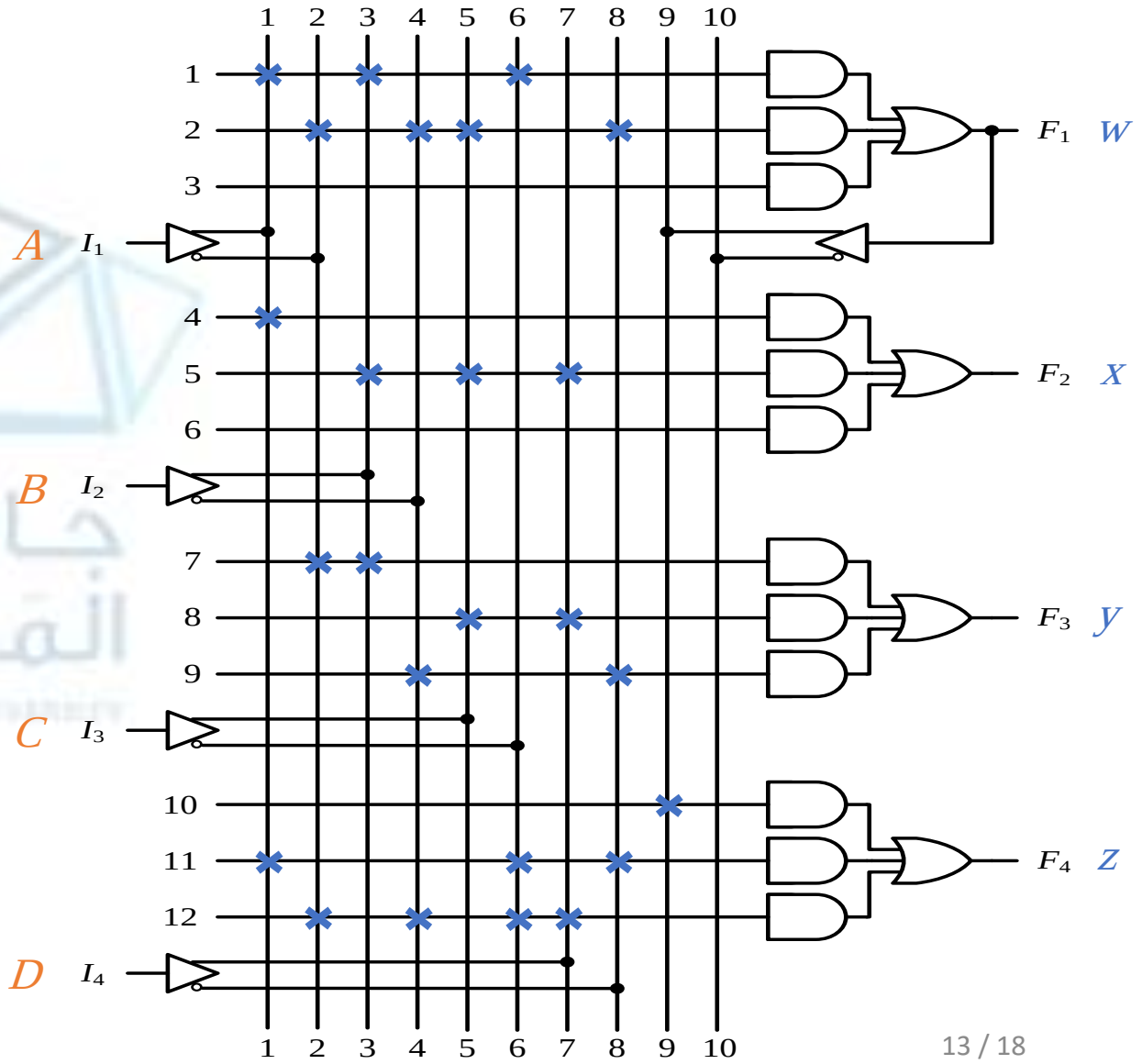
$w = ABC' + A'B'CD'$

$x = A + BCD$

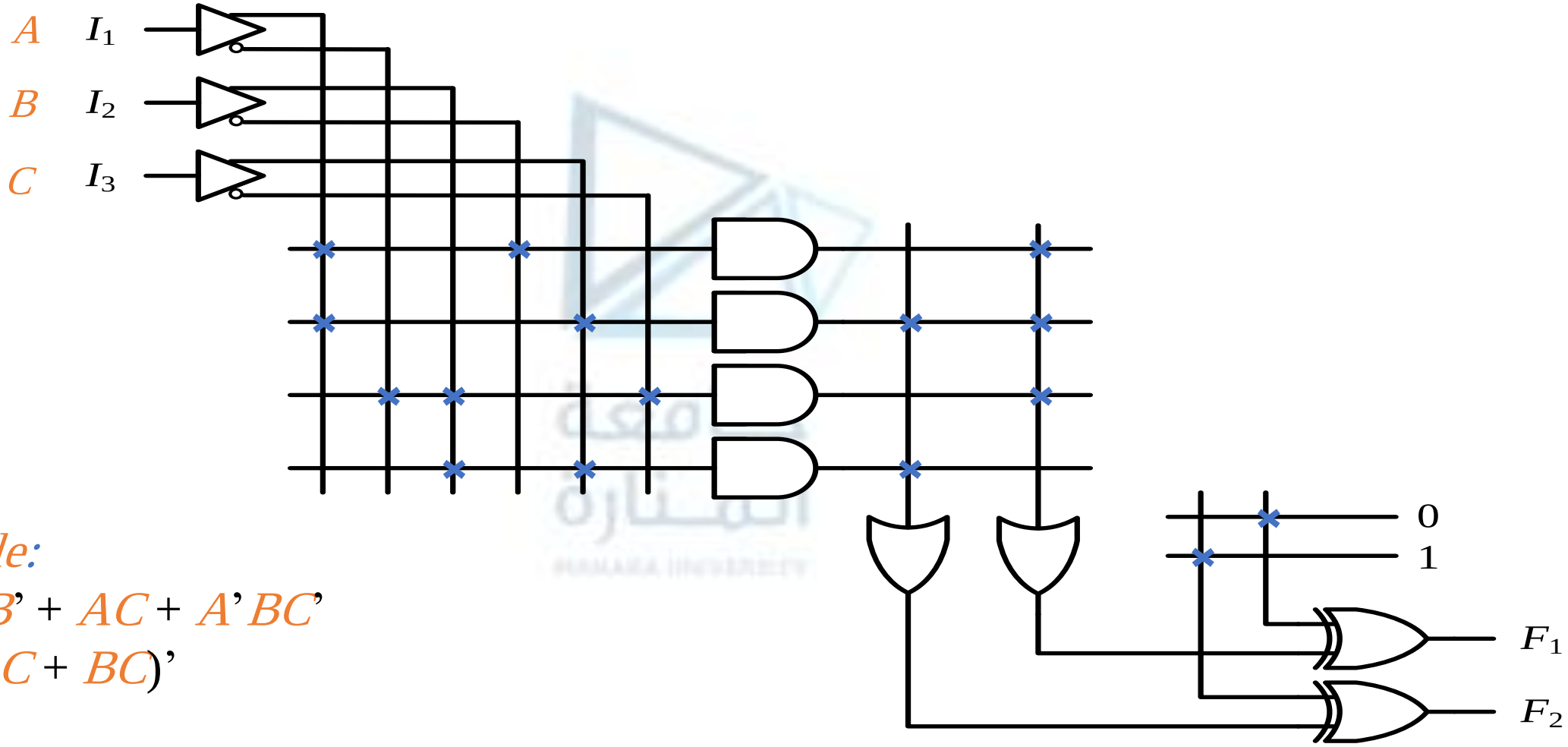
$y = A'B + CD + B'D'$

$z = ABC' + A'B'CD' + AC'D' + A'B'C'D$

$= w + AC'D' + A'B'C'D$



Programmable Logic Array (PLA)



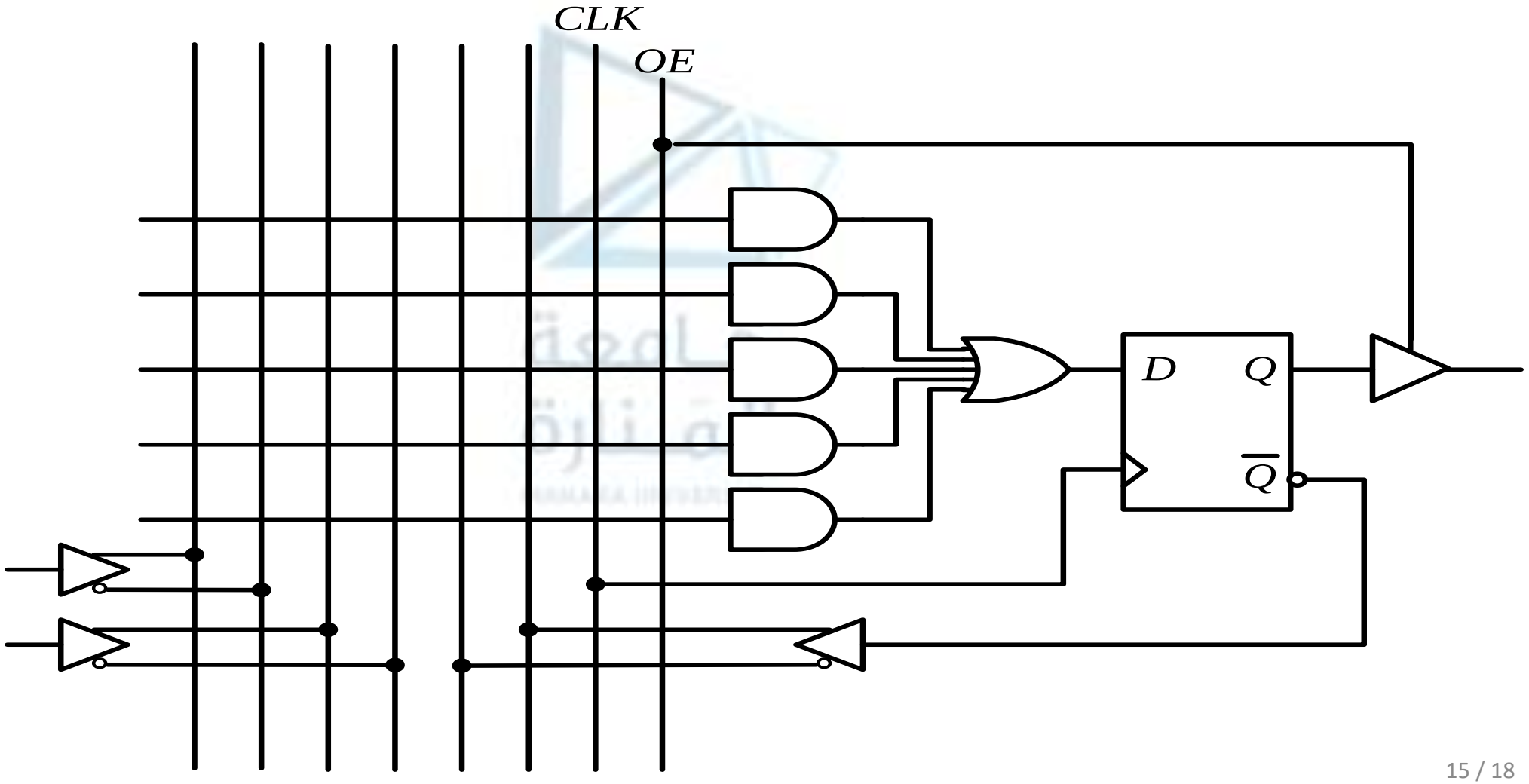
Example:

$F_1 = AB' + AC + A'BC'$

$F_2 = (AC + BC)'$

Sequential Programmable Logic Device

- Basic Macrocell Logic



Homework

- Mano
  - Chapter 7
    - 7-1
    - 7-2
    - 7-3
    - 7-18
    - 7-19

Homework

7-1 **The following memory units are specified by the number of words times the number of bits per word. How many address lines and input-output lines are needed in each case? (a) 4K × 16, (b) 2G × 8, (c) 16M × 32, (d) 256K × 64.**

7-2 **Give the number of bytes stored in the memories listed in Problem 7-1.**

7-3 **Word number 723 in a memory of 1024 × 16 contains the binary equivalent of 3,451. List the 10-bit address and the 16-bit memory content of the word.**

Homework

7-18 **Specify the size of a ROM (number of words and number of bits per word) that will accommodate the truth table for the following combinational circuit components:**

(a) a binary multiplier that multiplies two 4-bit,

(b) a 4-bit adder-subtractor,

(c) a quadruple 2-to-1-line multiplexers with common select and enable inputs, and

(d) a BCD-to-seven-segment decoder with an enable input.

Homework

7-19 **Tabulate the truth table for an 8 × 4 ROM that implements the Boolean functions**

$$A(x,y,z) = \sum(1,2,4,6)$$

$$B(x,y,z) = \sum(0,1,6,7)$$

$$C(x,y,z) = \sum(2,6)$$

$$D(x,y,z) = \sum(1,2,3,5,7)$$