

- Basic components
- The processor
 - * Execution cycle
 - * System clock
- Number of addresses
 - * 3-address machines
 - * 2-address machines
 - * 1-address machines
 - * 0-address machines
 - * Load/store architecture



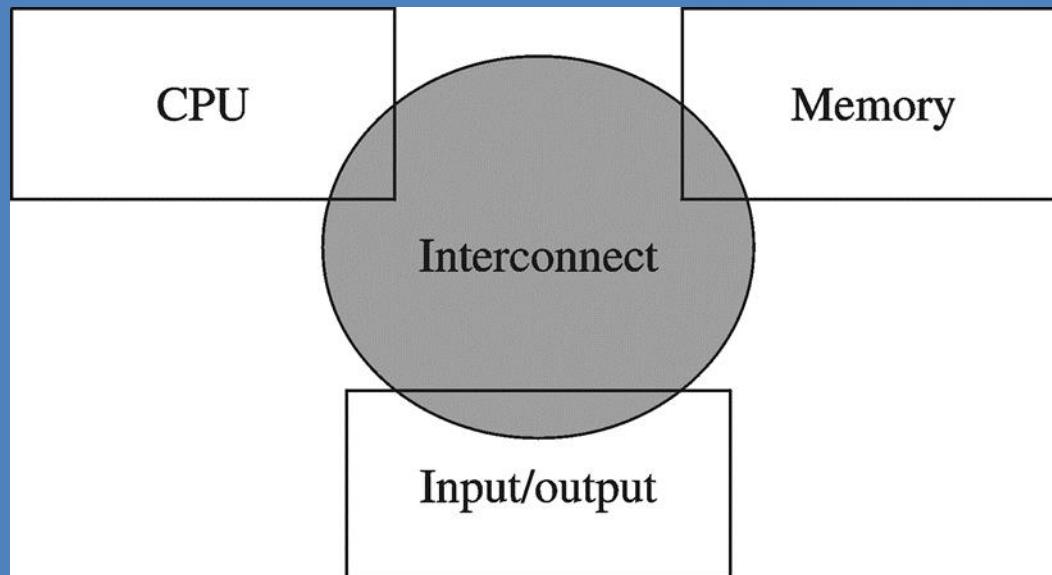
Basic Computer Organization

المكونات الأساسية للحاسوب

- Memory
 - * Basic operations
 - * Types of memory
 - * Storing multibyte data
- Input/Output

- Basic components of a computer system

- * Processor
- * Memory
- * I/O
- * System bus
 - » Address bus
 - » Data bus
 - » Control bus

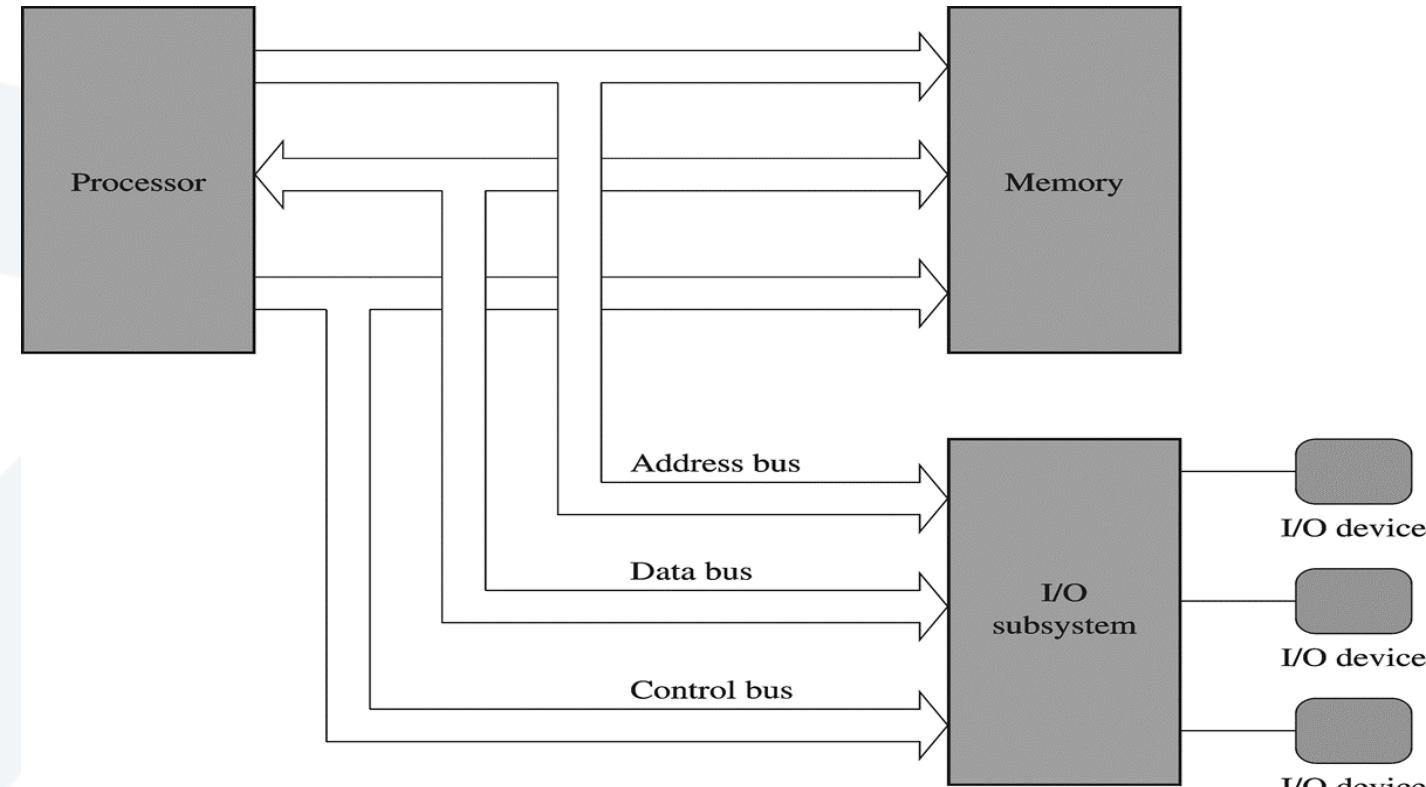
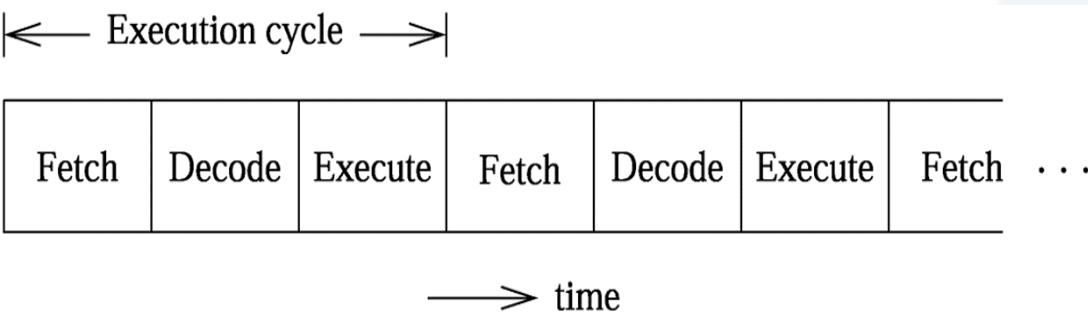


- * المعالج
- * الذاكر
- * وحدات الدخول / اخرج
- * خطوط النقل
- .. خطوط العنونة
- .. خطوط المعطيات
- .. خطوط التحكم

processor عمل المعالج

يقوم المعالج خلال دورة تنفيذ التعليمة بما يلي:

- مرحلة البحث عن التعليمة Fetch cycle
- مرحلة فك ترميز Decode
- مرحلة تنفيذ Execution



Number of Addresses

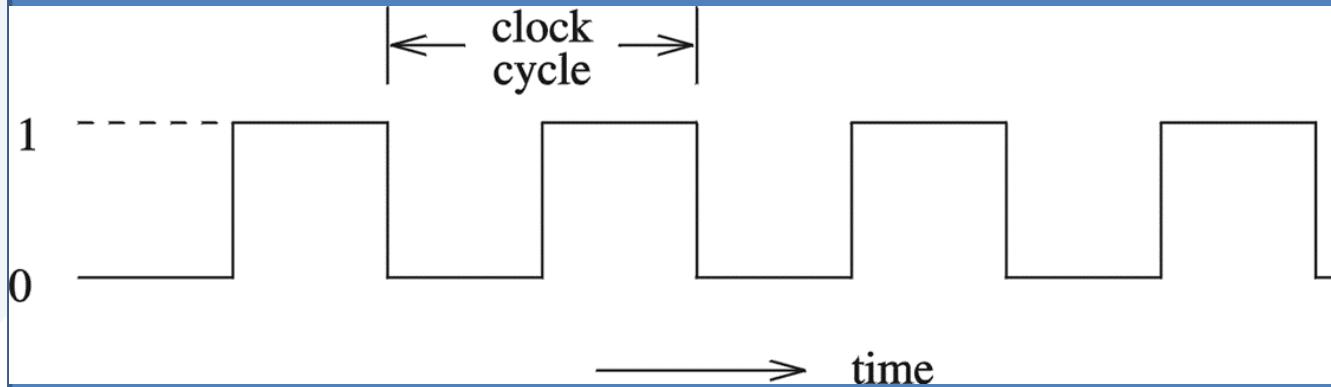
- Four categories
 - * 3-address machines
 - » 2 for the source operands and one for the result
 - * 2-address machines
 - » One address doubles as source and result
 - * 1-address machine
 - » Accumulator machines
 - » Accumulator is used for one source and result
 - * 0-address machines
 - » Stack machines
 - » Operands are taken from the stack
 - » Result goes onto the stack



The Processor

- System clock
 - * Provides timing signal

$$* \text{ Clock period} = \frac{1}{\text{Clock frequency}}$$



Number of Addresses

- Two-address machines
 - * One address doubles (for source operand & result)
 - * Last example makes a case for it
 - » Address T is used twice
 - * Sample instructions
- Three-address machines
 - * Two for the source operands, one for the result
 - * RISC processors use three addresses
 - * Sample instructions
 - add dest,src1,src2 ; $M(dest) = [src1] + [src2]$
 - sub dest,src1,src2 ; $M(dest) = [src1] - [src2]$
 - mult dest,src1,src2 ; $M(dest) = [src1] * [src2]$

Number of Addresses

- Zero-address machines

- * Stack supplies operands and receives the result
 - » Special instructions to load and store use an address
- * Called stack machines (Ex: HP3000, Burroughs B5500)
- * Sample instructions

push addr ; push([addr])

pop addr ; pop([addr])

add ; push(pop + pop)

sub ; push(pop - pop)

mult ; push(pop * pop)

- One-address machines

- * Uses special set of registers called accumulators
 - » Specify one source operand & receive the result
- * Called accumulator machines
- * Sample instructions

load addr ; accum = [addr]

store addr ; M[addr] = accum

add addr ; accum = accum + [addr]

sub addr ; accum = accum - [addr]

mult addr ; accum = accum * [addr]

الذواكر Memory



الذواكر
تبدو الذاكرة كنسق من البايت المتالية
لكل بايت عنوان
مثال تعنون الذاكرة من
 $0 \rightarrow 2^N - 1$

اذا كان عدد خطوط العنونة 32 bit
فيكون عدد مواقع الذاكرة
 $2^N - 1 = 4 G\ byte$

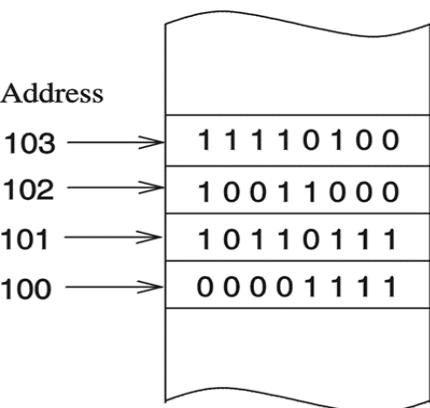
Address (in decimal)	Address (in hex)
$2^{32}-1$	FFFFFFF
	FFFFFEE
	FFFFFED
2	00000002
1	00000001
0	00000000

- Memory can be viewed as an ordered sequence of bytes
- Each byte of memory has an address
 - * Memory address is essentially the sequence number of the byte
 - * Such memories are called *byte addressable*
 - * Number of address lines determine the memory address space of a processor

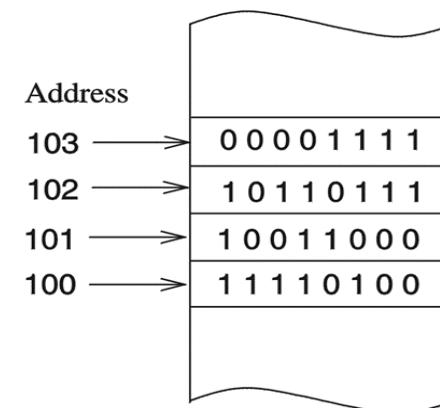
multibyte تخزين

MSB			LSB
1 1 1 1 0 1 0 0	1 0 0 1 1 0 0 0	1 0 1 1 0 1 1 1	0 0 0 0 1 1 1 1

(a) 32-bit data



(b) Little-endian byte ordering



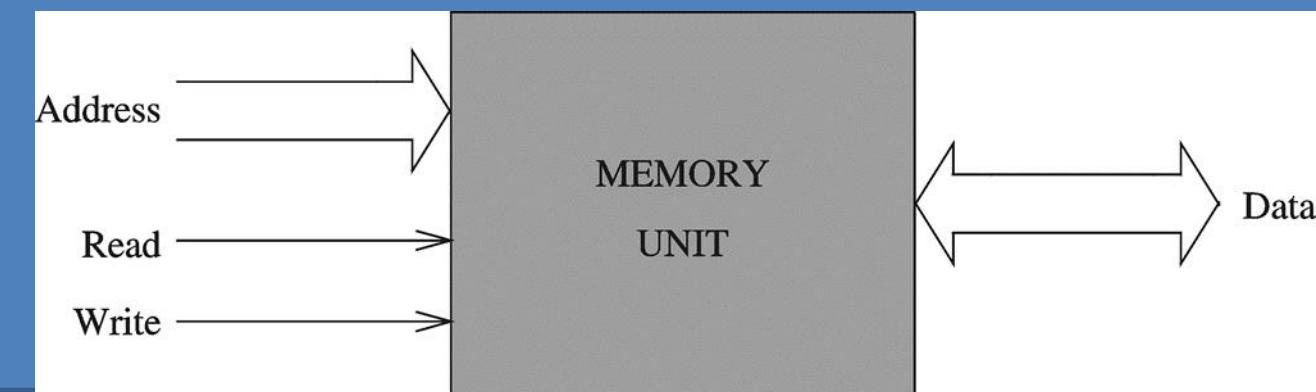
(c) Big-endian byte ordering

- **Little endian**
 - » Used by Intel IA-32 processors
- **Big endian**
 - » Used most processors by default



الذواكر Memory

- Two basic memory operations
 - * Read operation (read from memory)
 - * Write operation (write into memory)
- Access time
 - » Time needed to retrieve data at addressed location
- Cycle time
 - » Minimum time between successive operations



وحدات الدخول والخروج



وحدات الادخال والإخراج I/O

تستخدم بوابات الادخال والإخراج لتبادل المعطيات بين المعالج وبوابات الدخول / خرج يمكن تخطيط بوابات I/O كوحدة من الذاكرة

* تحجز بوابات الدخول / خرج عناوين من الذاكرة الرئيسية كما تفوم بعملية القراءة والكتابة كما في الذاكر

* بوابات دخل/خرج معزولة

- تستخدم فضاء عناوين منفصلة

- تحتاج الى تعليمات خاصة للدخل والخرج في معالجات بنتيوم مثل `in` , `out`

- تدعم معالجات انتل 80x68 وحدات دخل/خرج منفصلة

- Processor and I/O interface points for exchanging data are called *I/O ports*
- Two ways of mapping I/O ports
 - Memory-mapped I/O
 - I/O ports are mapped to the memory address space
 - Reading/writing I/O is similar to reading/writing memory
 - Can use memory read/write instructions
 - Isolated I/O
 - Separate I/O address space
 - Requires special I/O instructions (like `in` and `out` in Pentium)
 - Intel 80x86 processors support isolated I/O

عنونة I/O في معالجات بنتيوم

تستخدم معالجات بنتيوم فضاء العناوين

- تزود بفضاء عنوان 64 k byte

- يمكن ان تستخدم بوابات من 8 أو 16 أو 32

- تعليمات I/O لا تمر عبر المقاطع او الصفحات

- Pentium I/O address space

- * Provides 64 KB I/O address space
- * Can be used for 8-, 16-, and 32-bit I/O ports
- * Combination cannot exceed the total I/O address space
 - » can have 64 K 8-bit ports
 - » can have 32 K 16-bit ports
 - » can have 16 K 32-bit ports
 - » A combination of these for a total of 64 KB
- * I/O instructions do not go through segmentation or paging
 - » I/O address refers to the physical I/O address



