Lecture 9

(BJT BIASING)

طرق انحياز BJT

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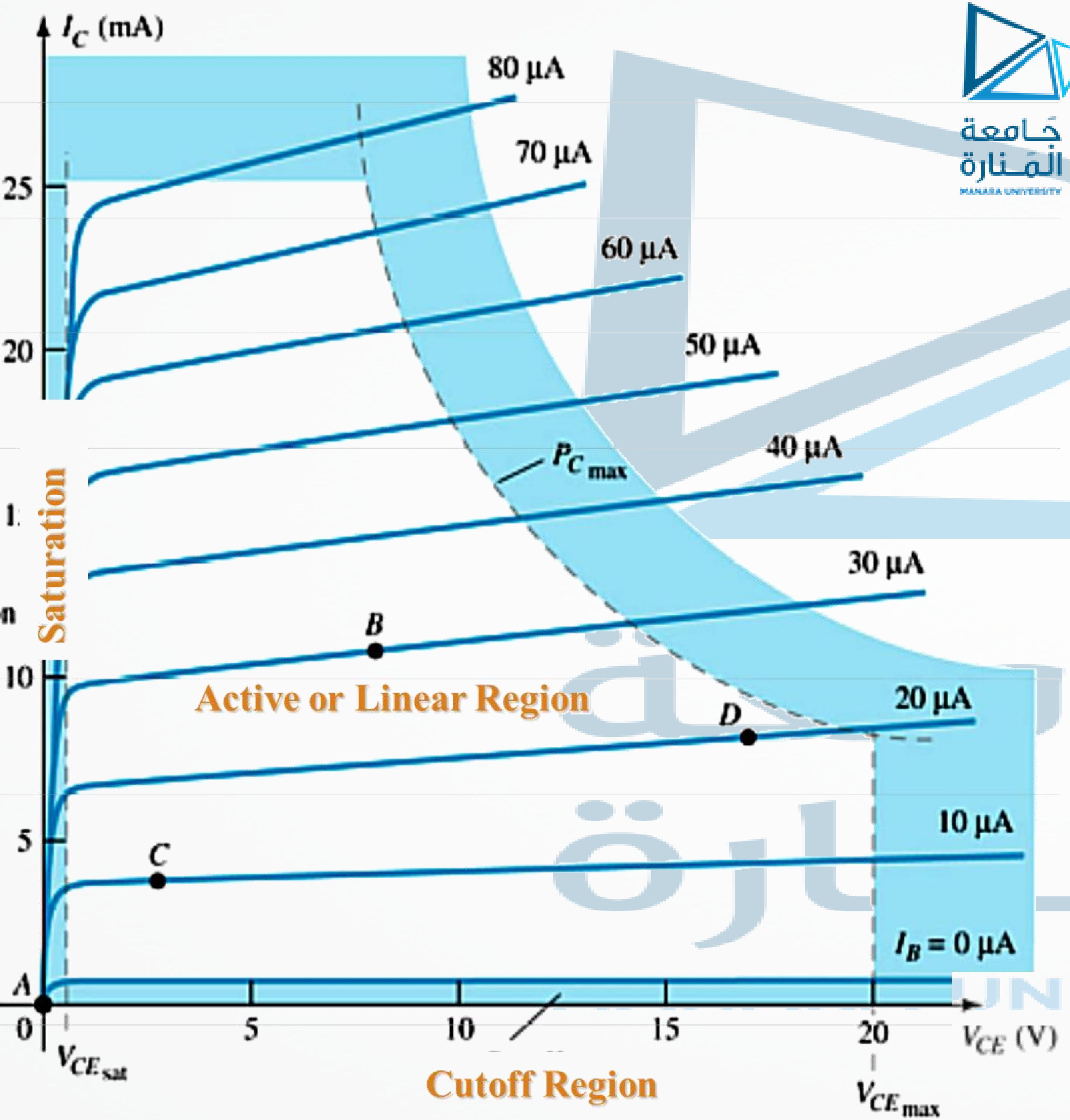


Biasing: The DC voltages applied to a transistor in order to turn it on so that it can amplify the AC signal.

- **Operating Point**

The DC input establishes an operating or quiescent point called the **Q-point**.

- **The Three States of Operation**

1. **Active or Linear Region Operation**

Base–Emitter junction is forward biased Base–Collector junction is reverse biased.

2. **Cutoff Region Operation**

Base–Emitter junction is reverse biased.

3. **Saturation Region Operation**

Base–Emitter junction is forward biased Base–Collector junction is forward biased.

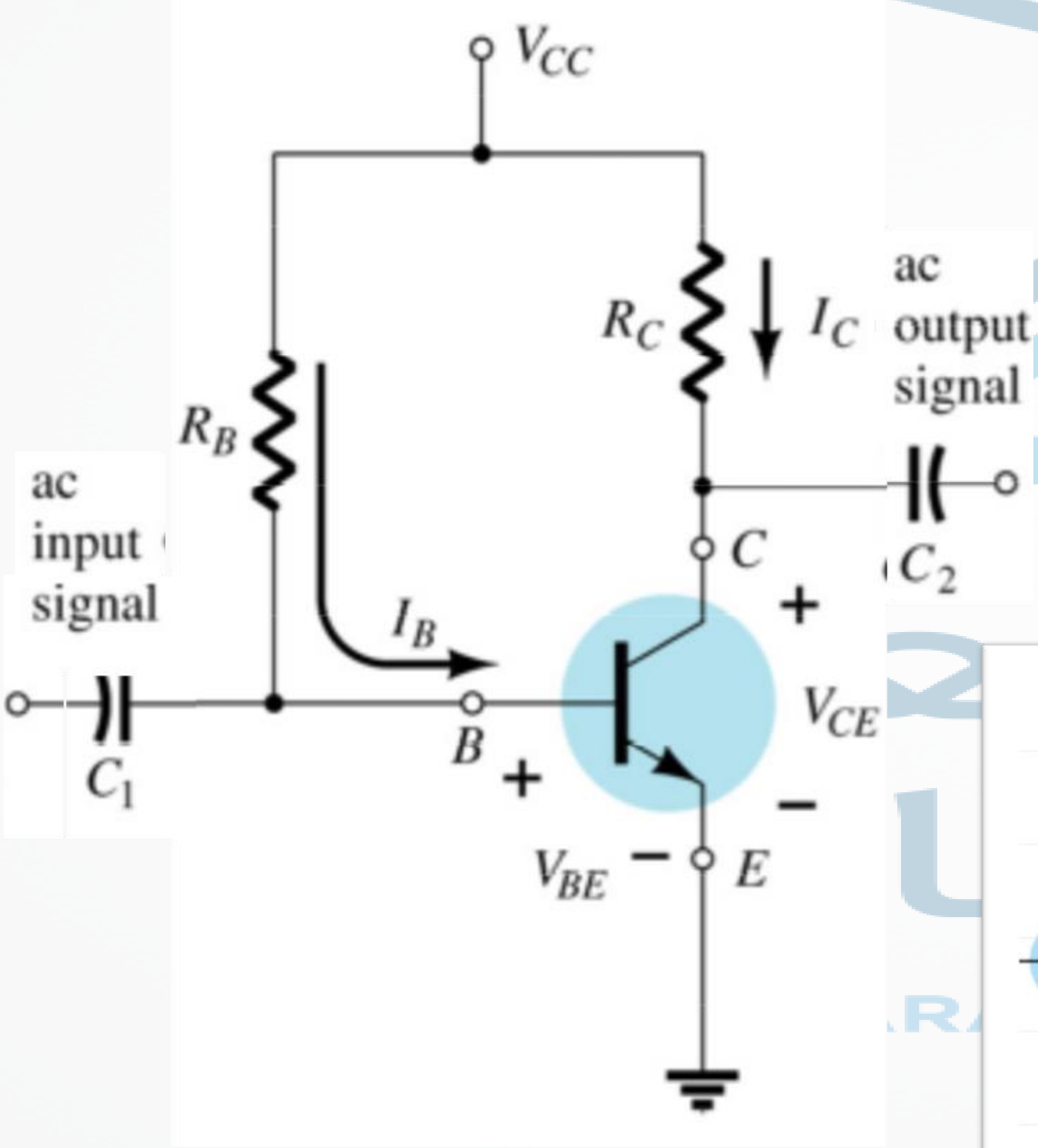
DC Biasing Circuits دارات الانحياز

- Fixed-bias circuit
- Emitter-stabilized bias circuit
- Collector-emitter loop
- Voltage divider bias circuit
- DC bias with voltage feedback

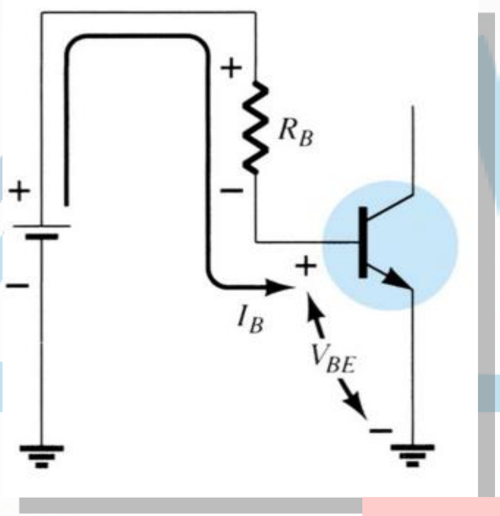
- دارة الانحياز الثابت
- دارة انحياز الباعث المستقر
- دارة الانحياز لحلقة الباعث المجمع
- دارة انحياز مجزئ الجهد
- دارة الانحياز بالتغذية العكسية

Fixed-bias circuit

دارة الانحياز الثابت



- **The Base-Emitter Loop**



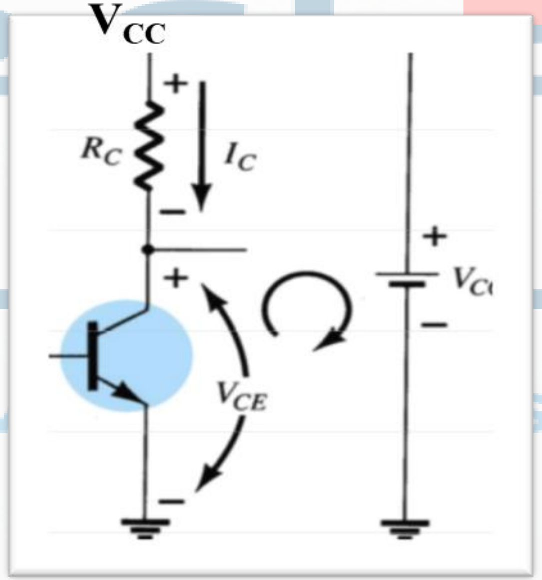
From Kirchhoff's voltage law:

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Solving for base current:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

- **Collector-Emitter Loop**



Collector current:

$$I_C = \beta I_B$$

From Kirchhoff's voltage law:

$$V_{CE} = V_{CC} - I_C R_C$$

Load Line Analysis

- **Active or Linear Region**

The Q-point is the operating point:

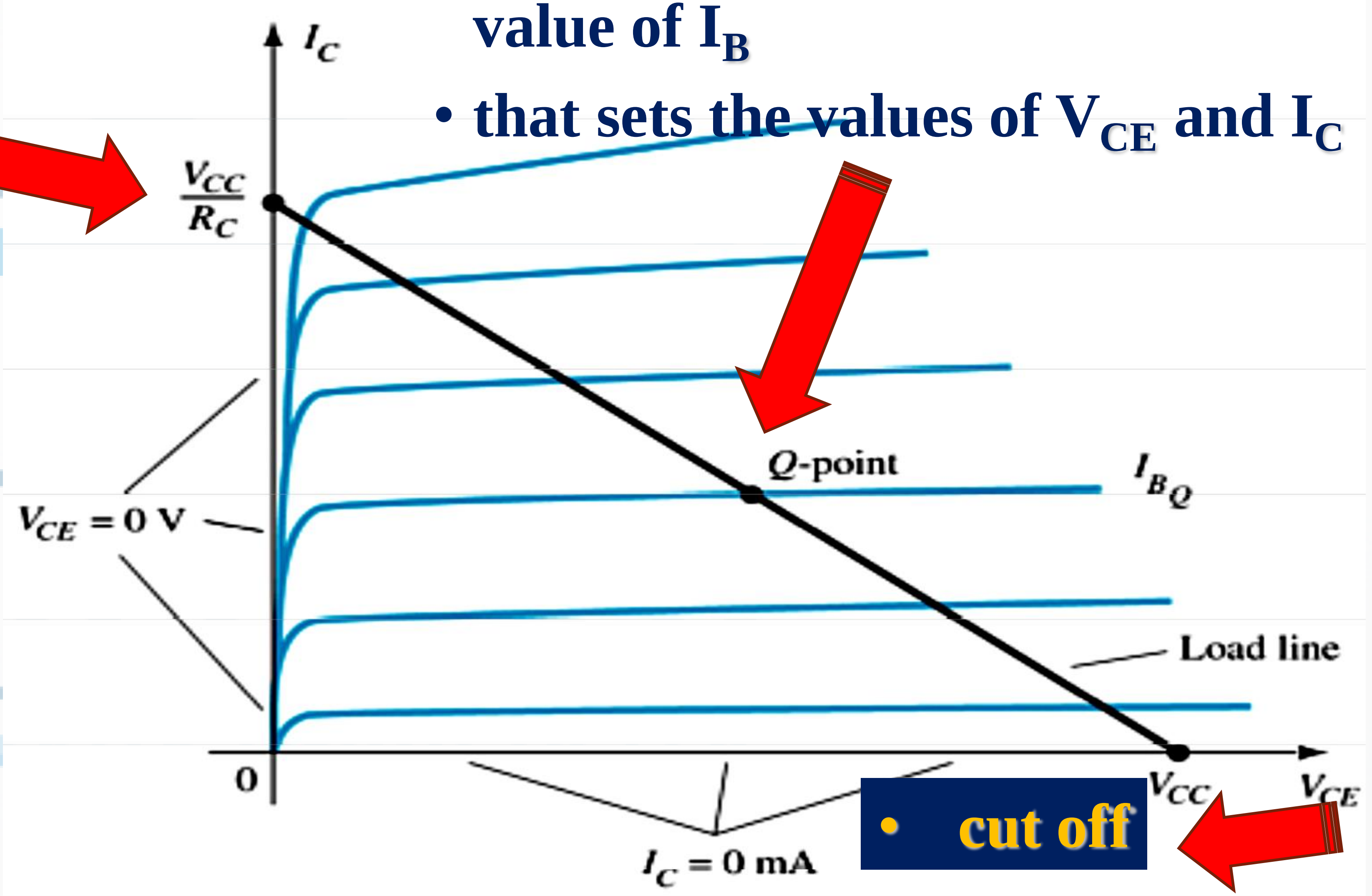
- where the value of R_B sets the value of I_B
- that sets the values of V_{CE} and I_C

- **Saturation**

When the transistor is operating in saturation, current through the transistor is at its maximum possible value.

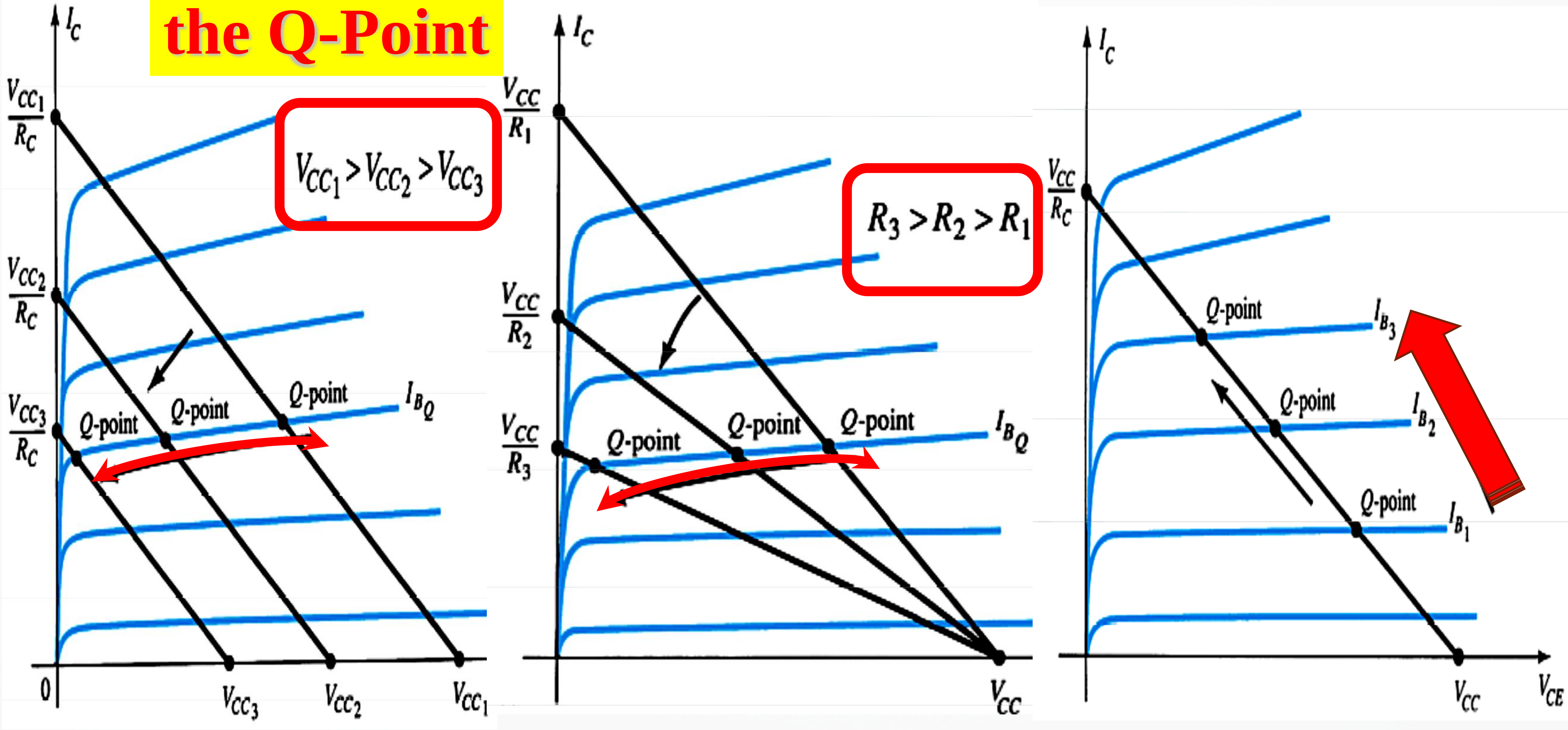
$V_{CE} \cong 0\,V$

$$I_{Csat} = \frac{V_{CC}}{R_C}$$

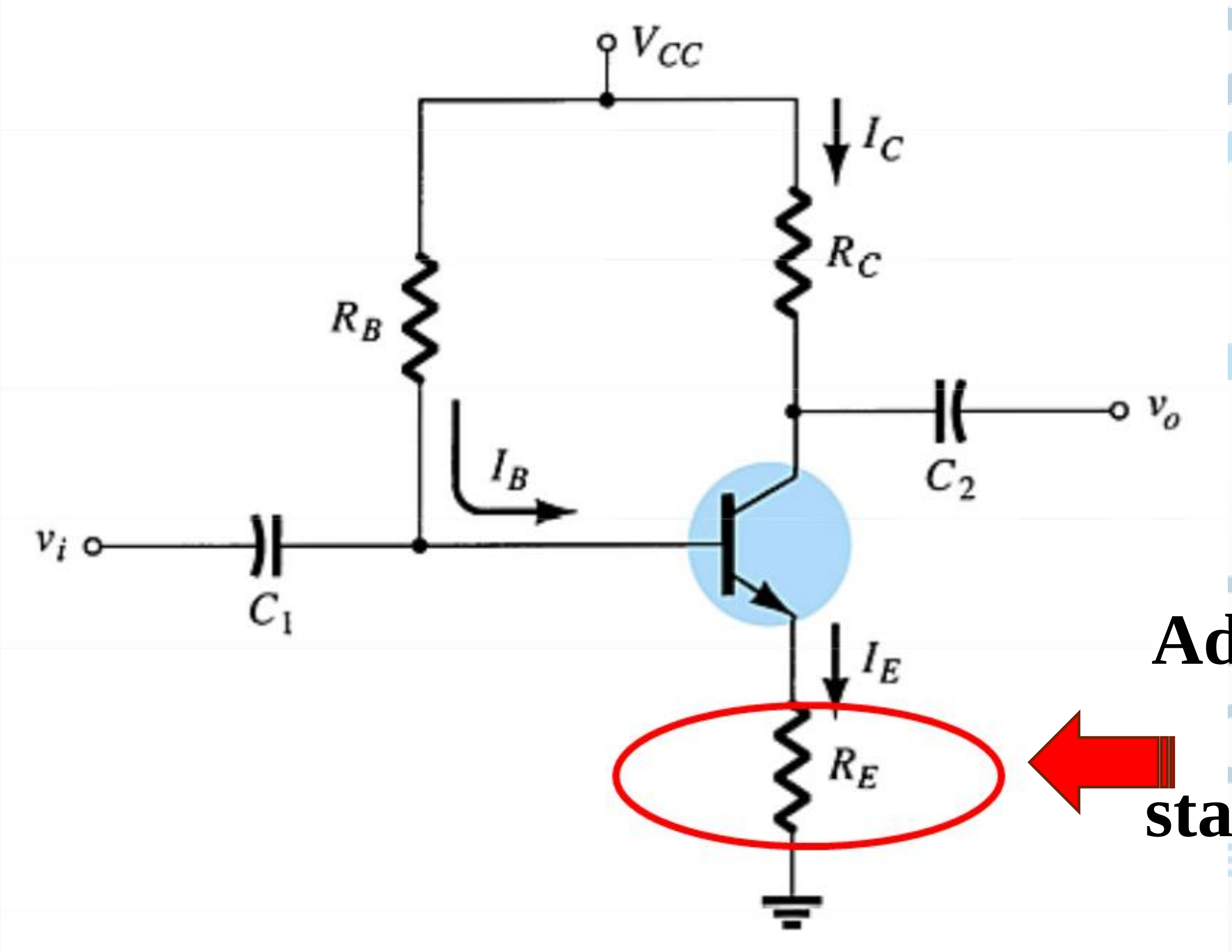


- **cut off**

Circuit Values Affect the Q-Point



Emitter-Stabilized Bias Circuit



Adding a resistor (R_E) to the emitter circuit stabilizes the bias circuit. circuit.

Base-Emitter Loop

From Kirchhoff's voltage law:

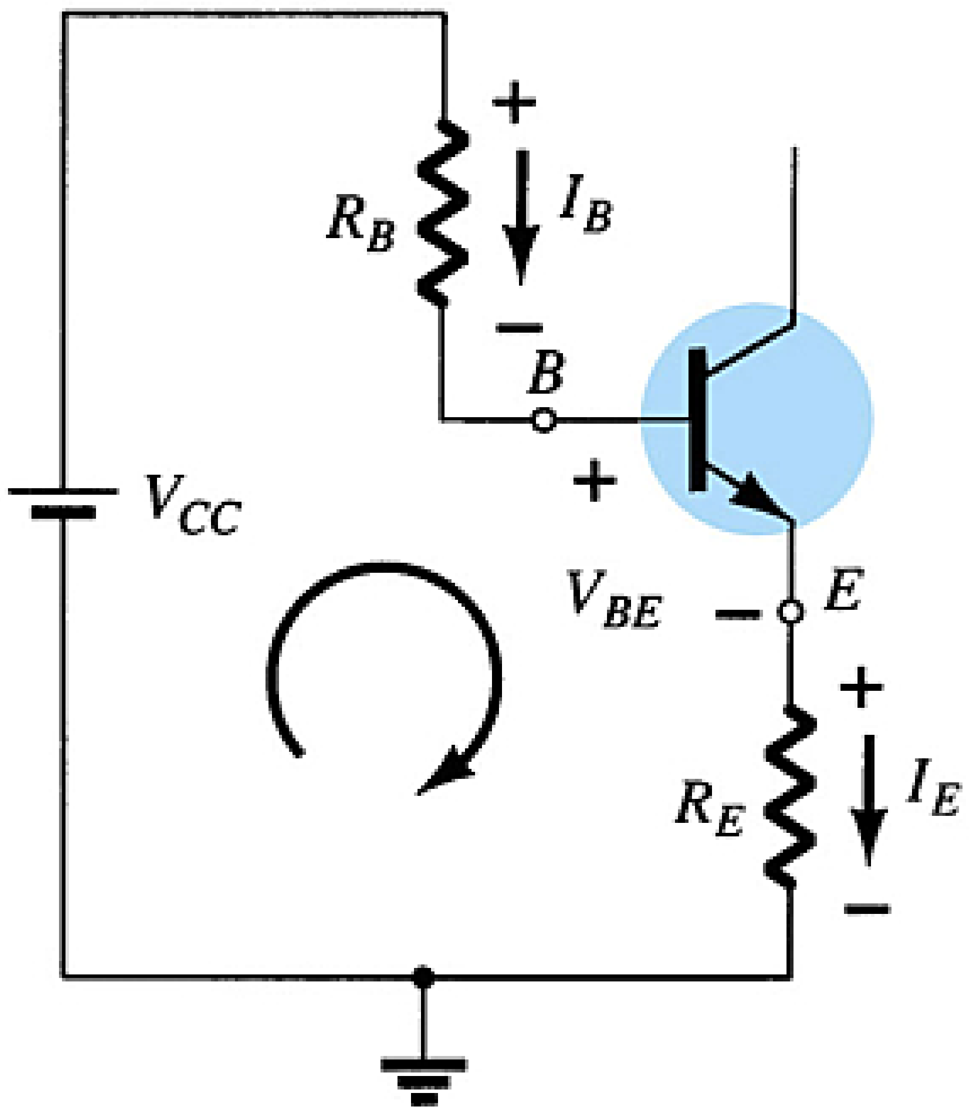
$$+V_{CC} - I_E R_E - V_{BE} - I_E R_E = 0$$

Since $I_E = (\beta + 1)I_B$:

$$V_{CC} - I_B R_B - (\beta + 1) I_B R_E = 0$$

Solving for IB:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$



Collector-Emitter Loop

From Kirchhoff's voltage law:

$$I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Since $I_E \cong I_C$:

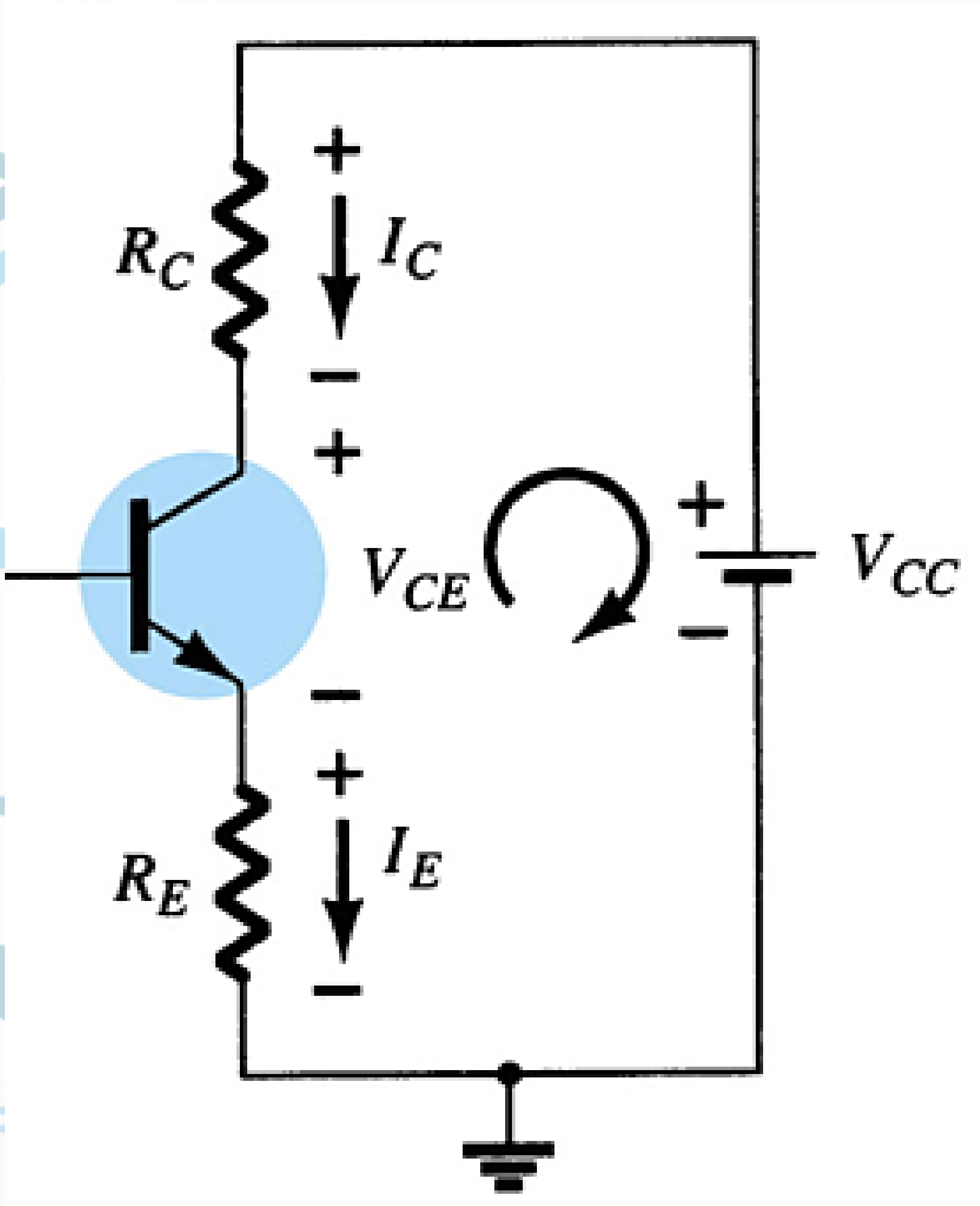
$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Also:

$$V_E = I_E R_E$$

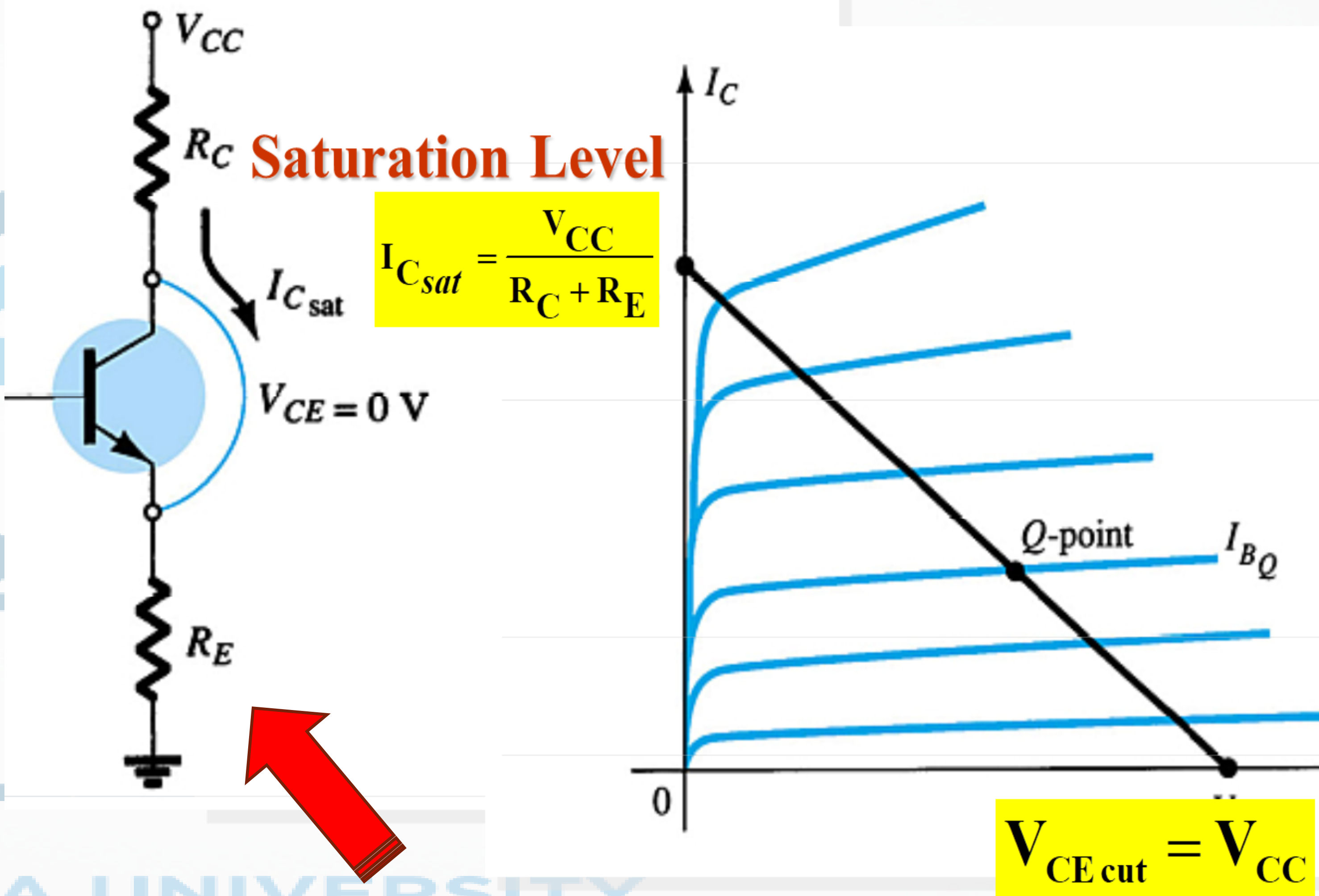
$$V_C = V_{CE} + V_E = V_{CC} - I_C R_C$$

$$V_B = V_{CC} - I_R R_B = V_{BE} + V_E$$



Improved Biased Stability

Stability **refers to a circuit condition in which the currents and voltages will remain fairly constant over a wide range of temperatures and transistor Beta (β) values.**



Adding Re to the emitter improves the stability of a transistor.

Voltage Divider Bias

This is a very stable bias circuit.
The currents and voltages are nearly independent of any variations in β.

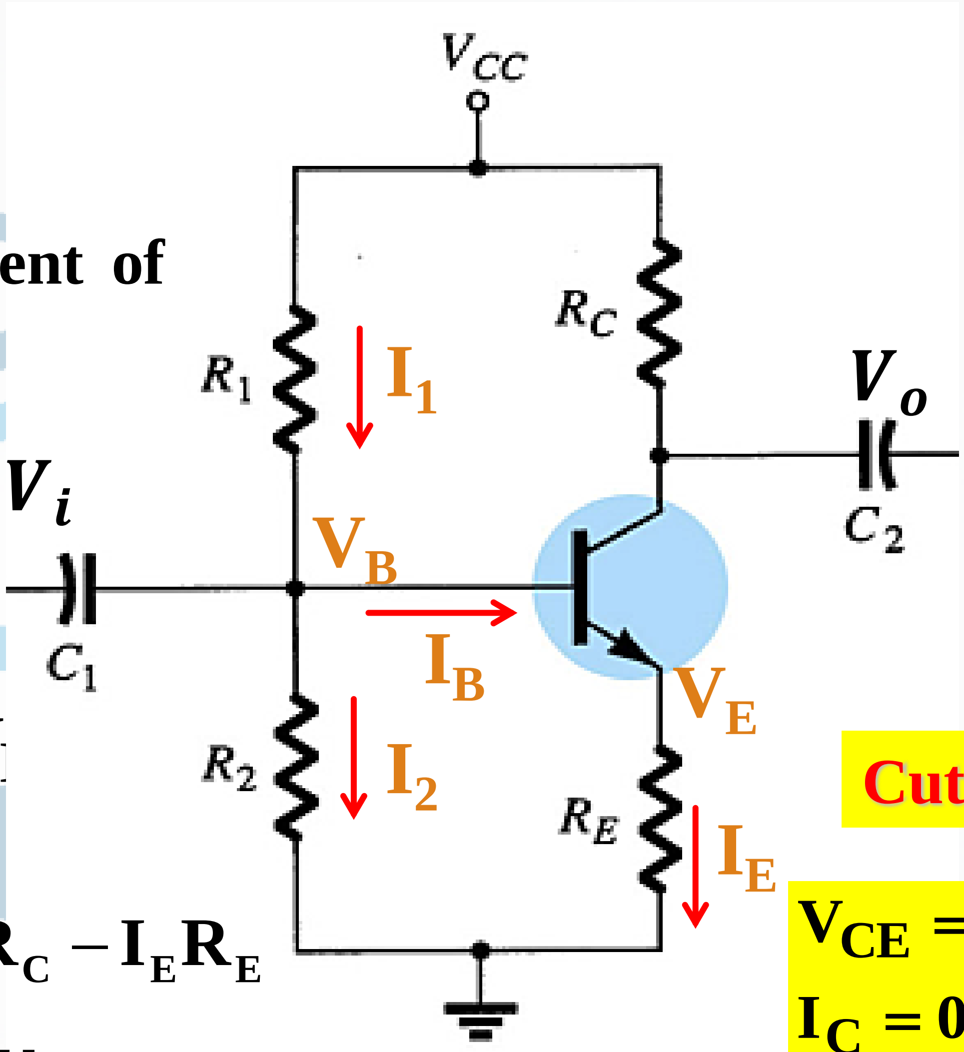
Approximate Analysis

Where $I_B << I_1$ and $I_1 \cong I_2$:

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Where $\beta R_E > 10R_2$:

$$I_E = \frac{V_E}{R_E} \qquad V_E = V_B - V_{BE}$$



From Kirchhoff's voltage law: $V_{CE} = V_{CC} - I_C R_C - I_E R_E$

Transistor Saturation Level $I_{Csat} = I_{Cmax} = \frac{V_{CC}}{R_C + R_E}$

Load Line Analysis $I_E \cong I_C$ $\qquad V_{CE} = V_{CC} - I_C(R_C + R_E)$

Cutoff:

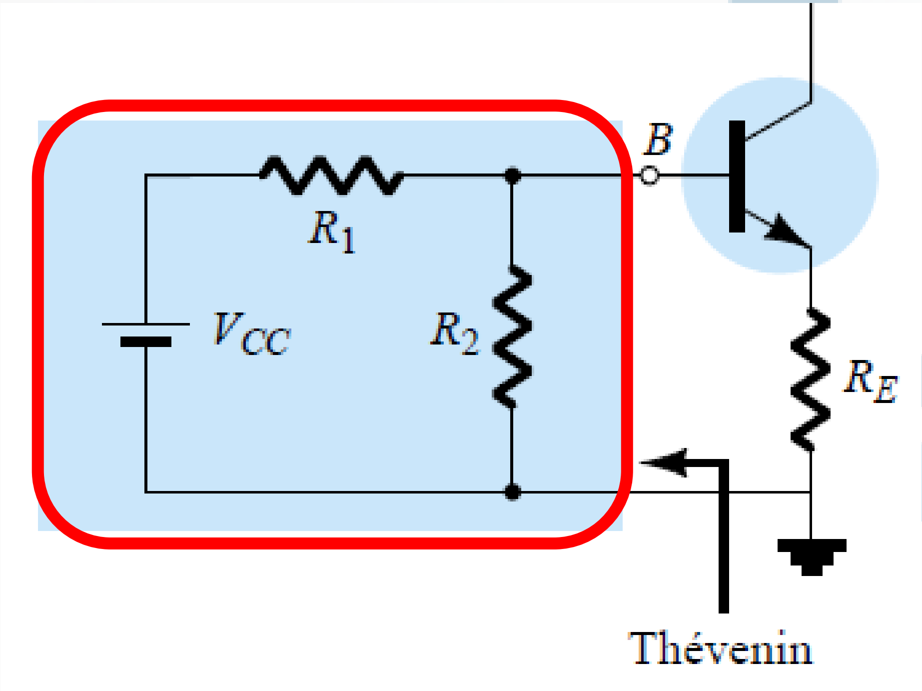
$V_{CE} = V_{CC}$

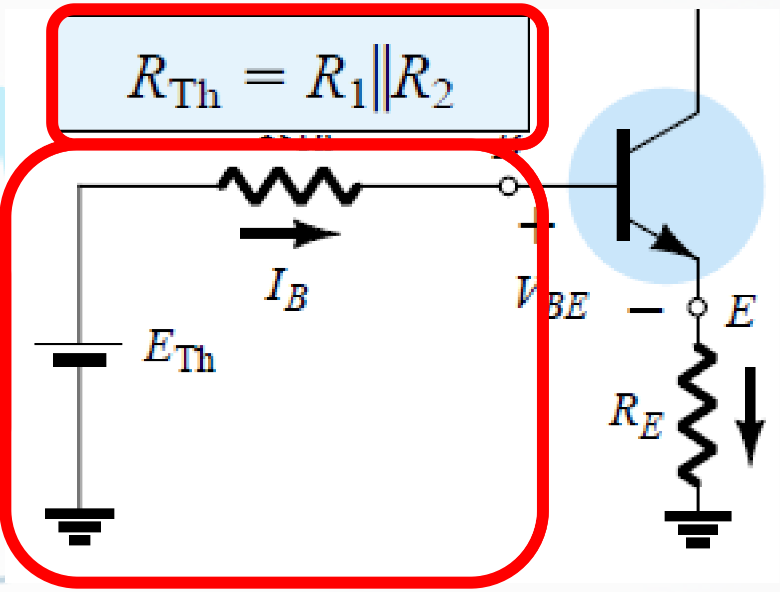
$I_C = 0mA$

Saturation:

$$I_C = \frac{V_{CC}}{R_C + R_E}$$

$V_{CE} = 0V$





$$R_{Th} = R_1 \| R_2$$

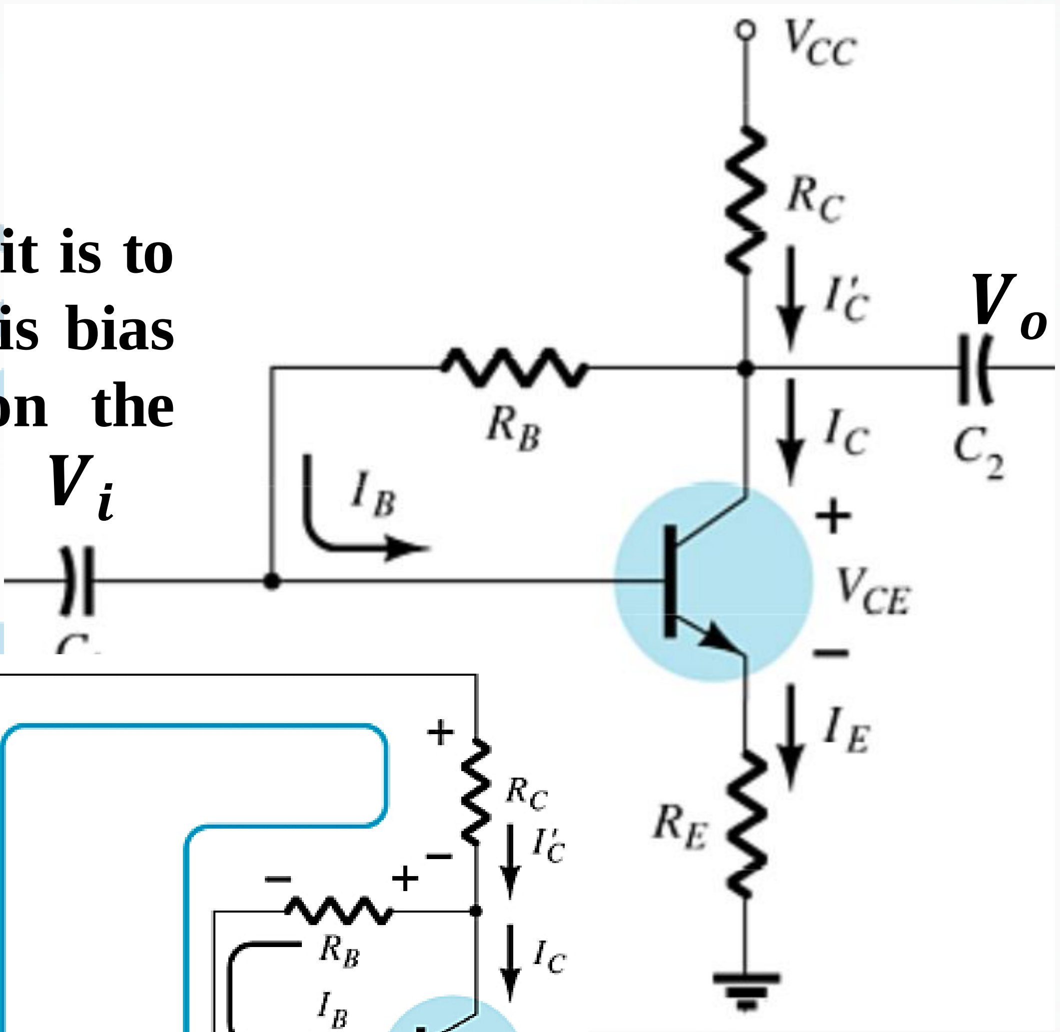
$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

DC Bias with Voltage Feedback

Another way to improve the stability of a bias circuit is to add a feedback path from collector to base. In this bias circuit the Q-point is only slightly dependent on the transistor beta, β.



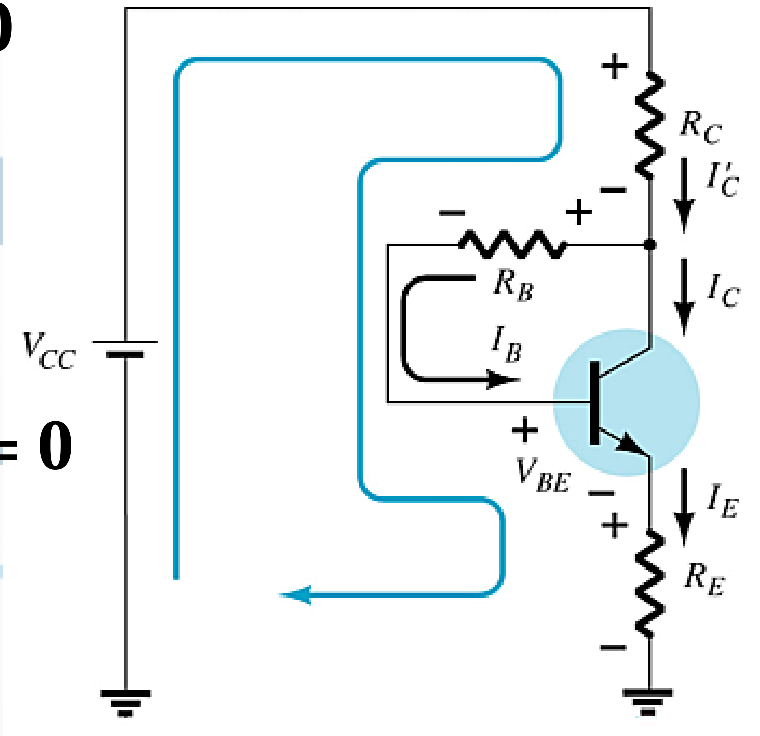
From Kirchhoff's voltage law:

$$V_{CC} - I'_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

Where $I_B << I_C$: $I'_C = I_C + I_B \cong I_C$

Knowing $I_C = \beta I_B$ and $I_E \cong I_C$, :

$$V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$



Solving for I_B:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

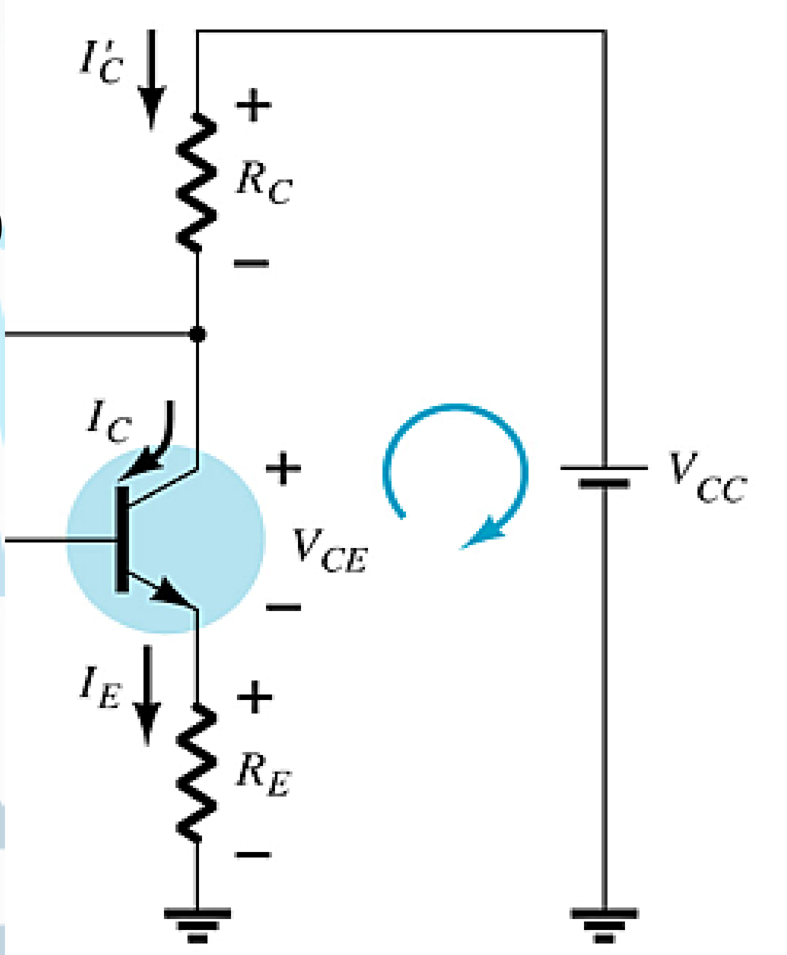
Collector-Emitter Loop

Applying Kirchoff's voltage law: $I_E + V_{CE} + I'_C R_C - V_{CC} = 0$

Since $I'_C \cong I_C$ and $I_C = \beta I_B$: $I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$

Solving for V_{CE}: $V_{CE} = V_{CC} - I_C(R_C + R_E)$

Transistor Saturation Level $I_{Csat} = I_{Cmax} = \dfrac{V_{CC}}{R_C + R_E}$



Load Line Analysis

Cutoff:

$$V_{CE} = V_{CC}$$

$$I_C = 0\ mA$$

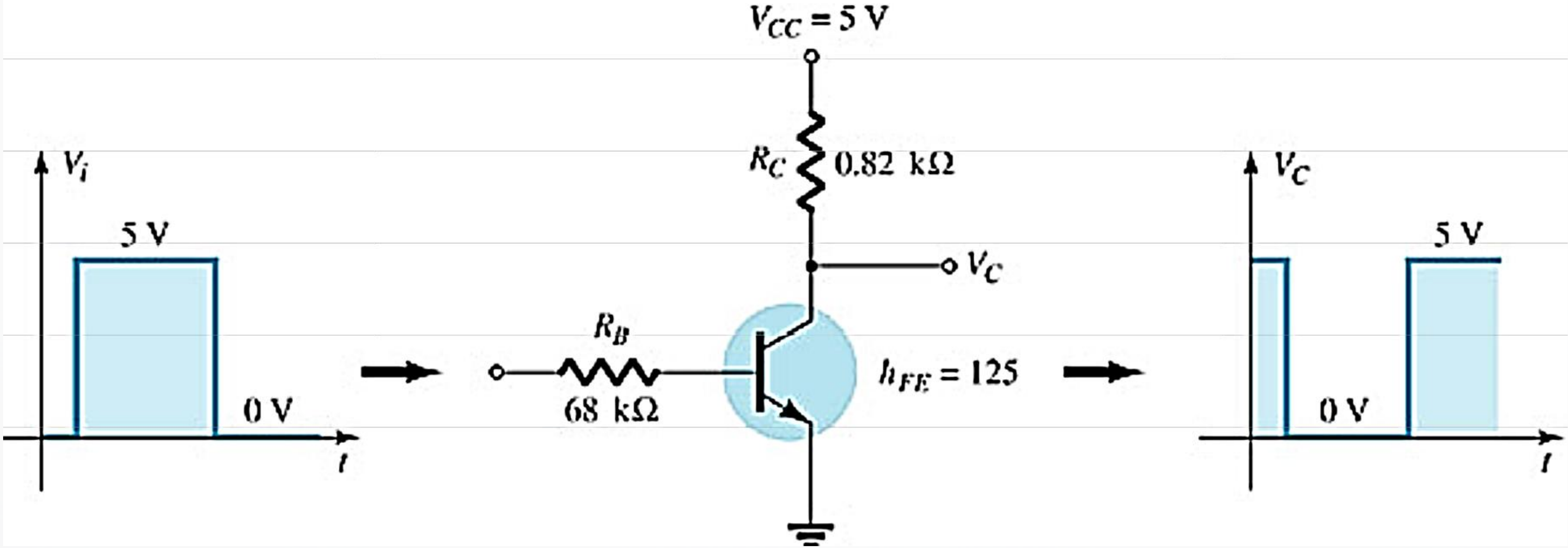
Saturation:

$$I_C = \frac{V_{CC}}{R_C + R_E}$$

$$V_{CE} = 0\ V$$

Transistor Switching Networks

Transistors with only the DC source applied can be used as electronic switches.



Switching Circuit Calculations

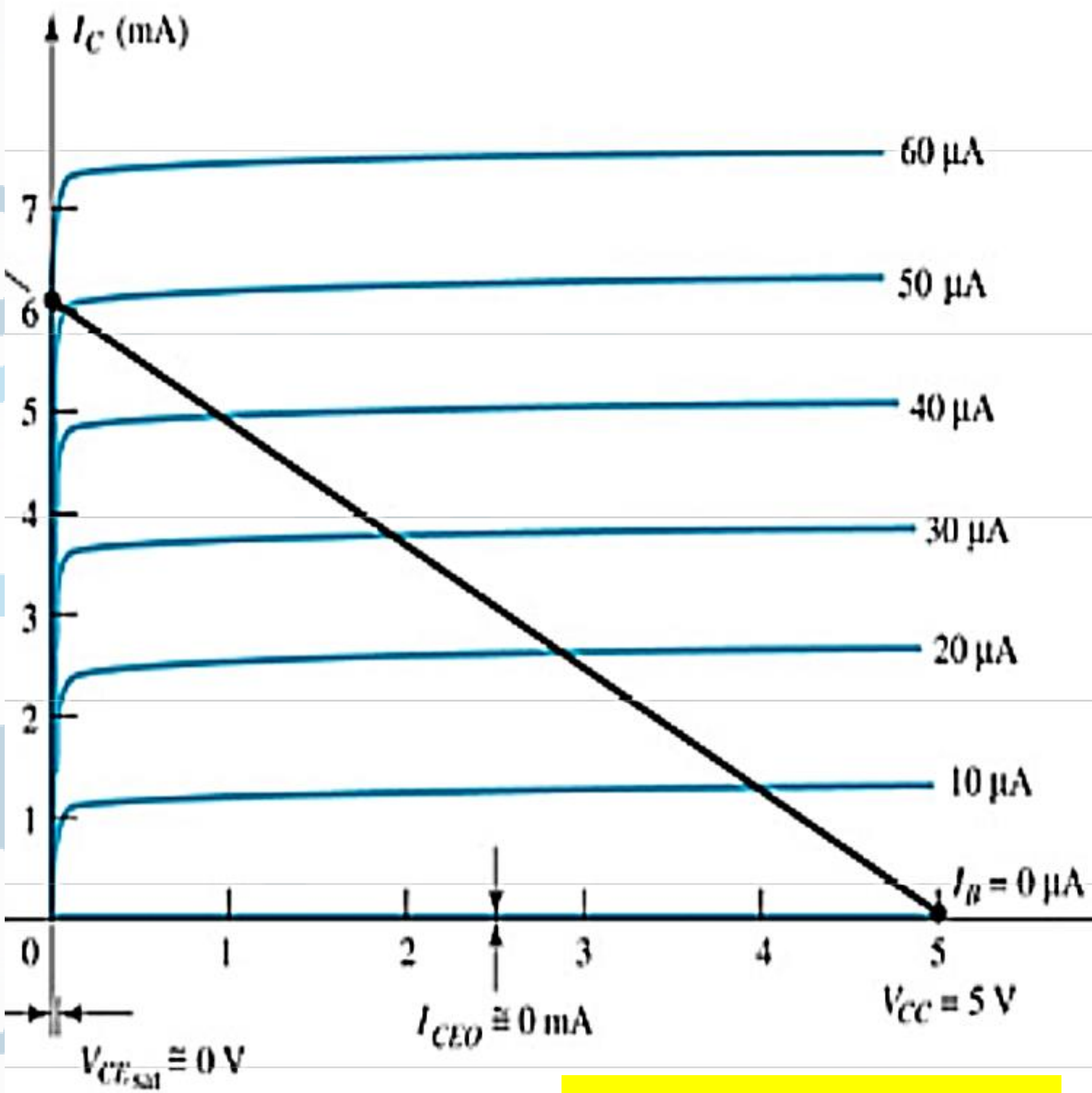
resistance at saturation $R_{sat} = \frac{V_{CEsat}}{I_{Csat}}$

Saturation current:

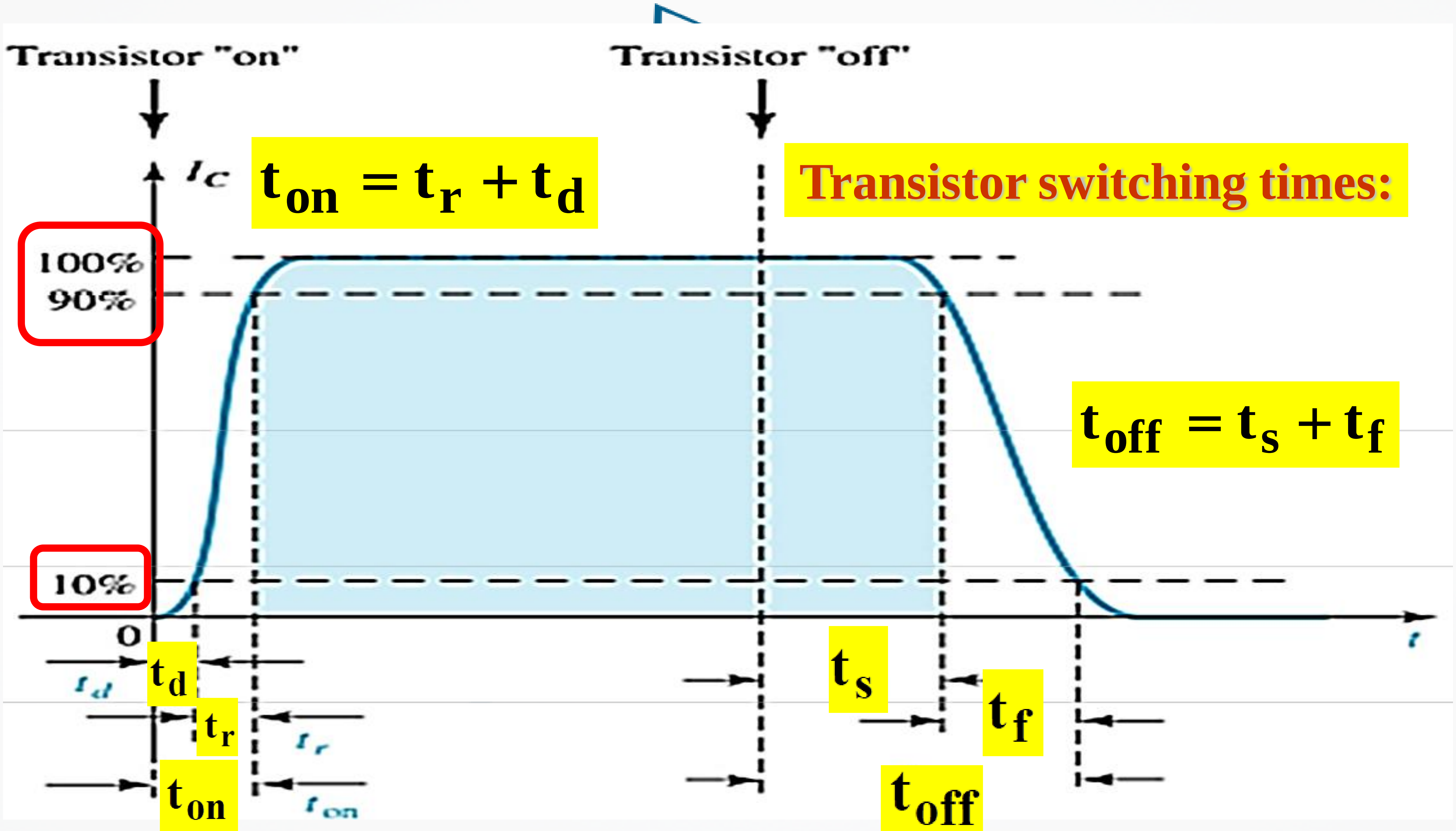
$$I_{Csat} = \frac{V_{CC}}{R_C}$$

To ensure saturation:

$$I_B > \frac{I_{Csat}}{\beta_{dc}}$$



resistance at cutoff $R_{cutoff} = \frac{V_{CC}}{I_{CEO}}$



Transistor switching times:
$t_{on} = t_r + t_d$
$t_{off} = t_s + t_f$
Transistor "on"
Transistor "off"
I_C
100%
90%
10%
0
t
t_d
t_r
t_{on}
t_s
t_f
t_{off}

PNP Transistors

The analysis for ***pnp*** transistor biasing circuits is the same as that for ***npn*** transistor circuits. The only difference is that the currents are flowing in the opposite direction.