Lecture 4

Boolean Algebra

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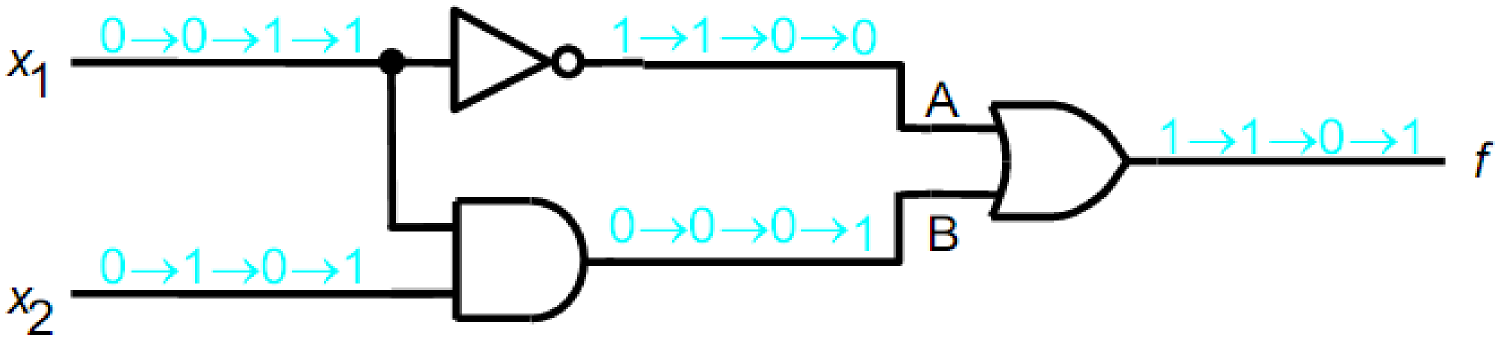
Timing diagram

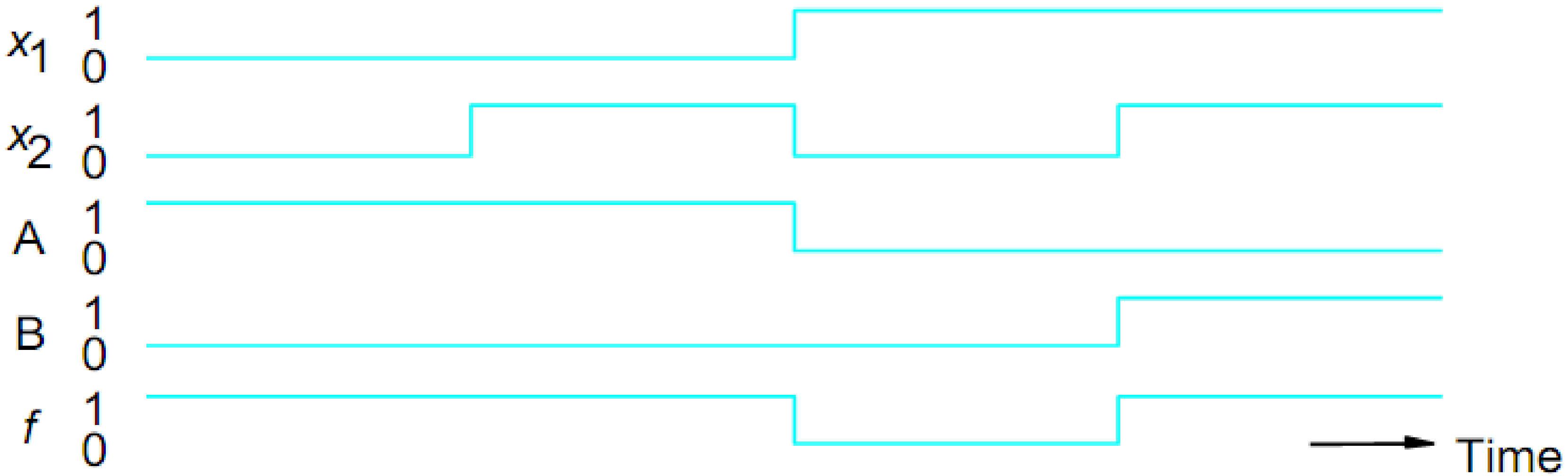


(a) Network that implements $f = x_1' + x_1 \cdot x_2$

x_1	x_2	$f(x_1, x_2)$
0	0	1
0	1	1
1	0	0
1	1	1

A	B
1	0
1	0
0	0
0	1

(b) Truth table



(c) Timing diagram

Boolean

Axioms of Boolean Algebra

A1)	$0 \cdot 0 = 0$	A1')	$1 + 1 = 1$
A2)	$1 \cdot 1 = 1$	A2')	$0 + 0 = 0$
A3)	$0 \cdot 1 = 1 \cdot 0 = 0$	A3')	$1 + 0 = 0 + 1 = 1$
A4)	if $x = 0$, then $x' = 1$	A4')	if $x = 1$, then $x' = 0$

- **Single variable theorems**

T1) $x \cdot 0 = 0$

T1') $x + 1 = 1$

T2) $x \cdot 1 = x$

T2') $x + 0 = x$

T3) $x \cdot x = x$

T3') $x + x = x$

T4) $x \cdot x' = 0$

T4') $x + x' = 1$

T5) $x'' = x$

- **Two and three variable theorems**

T6) $x \cdot y = y \cdot x$

T6') $x + y = y + x$

T7) $x \cdot (y \cdot z) = (x \cdot y) \cdot z$

T7') $x + (y + z) = (x + y) + z$

T8) $x \cdot (y + z) = x \cdot y + x \cdot z$

T8') $x + y \cdot z = (x + y) \cdot (x + z)$

T9) $x + x \cdot y = x$

T9') $x \cdot (x + y) = x$

T10) $x \cdot y + x \cdot y' = x$

T10') $(x + y) \cdot (x + y') = x$

T11) $(x \cdot y)' = x' + y'$

T11') $(x + y)' = x' \cdot y'$

T12) $x + x' \cdot y = x + y$

T12') $x \cdot (x' + y) = x \cdot y$

T13) $x \cdot y + y \cdot z + x' \cdot z = x \cdot y + x' \cdot z$

T13') $(x + y) \cdot (y + z) \cdot (x' + z) = (x + y) \cdot (x' + z)$

Example: Apply theorems of Boolean Algebra to prove that the left and right hand sides of the following logic equation are identical.

$$x_1 \cdot x_3' + x_2' \cdot x_3' + x_1 \cdot x_3 + x_2' \cdot x_3 = x_1' \cdot x_2' + x_1 \cdot x_2 + x_1 \cdot x_2'$$

- **The Venn Diagram**

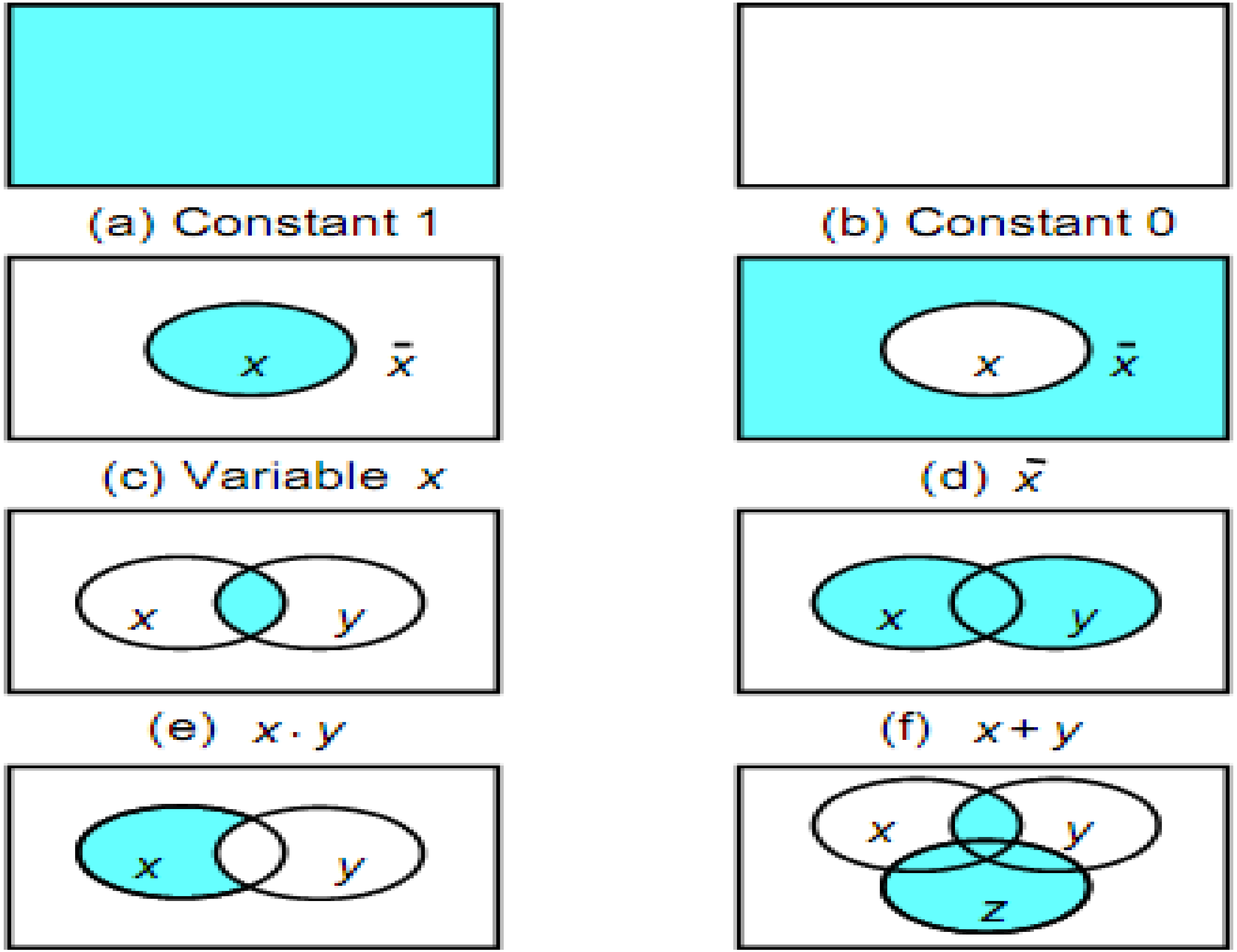
– Graphical illustration of various operations and relations in the algebra of sets

– A set s is a collection of elements that are said to be members of s

– In Venn diagram the elements of a set are represented by the area enclosed by a square, circle or ellipse

– In Boolean algebra there are only two elements in the universe, i.e. {0,1}. Then the area within a contour corresponding to a set s denotes that s = 1, while the area outside the contour denotes s = 0

– In a Venn diagram we shade the area where s = 1



(a) Constant 1

(b) Constant 0

(c) Variable x

(d) $\bar{x}$

(e) $x \cdot y$

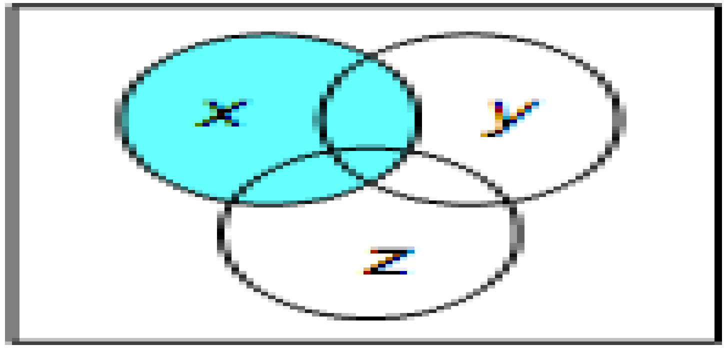
(f) $x + y$

(g) $x \cdot \bar{y}$

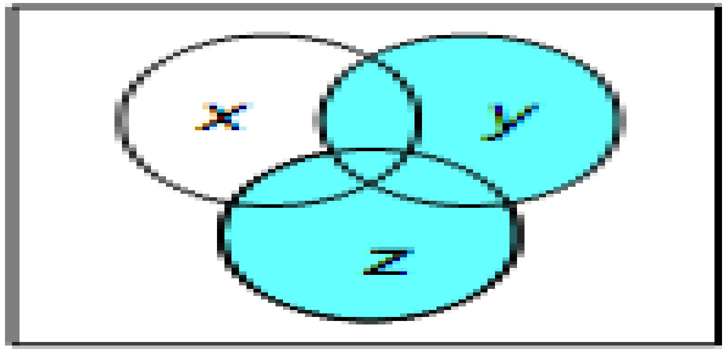
(h) $x \cdot y + z$

The Venn diagram representation.

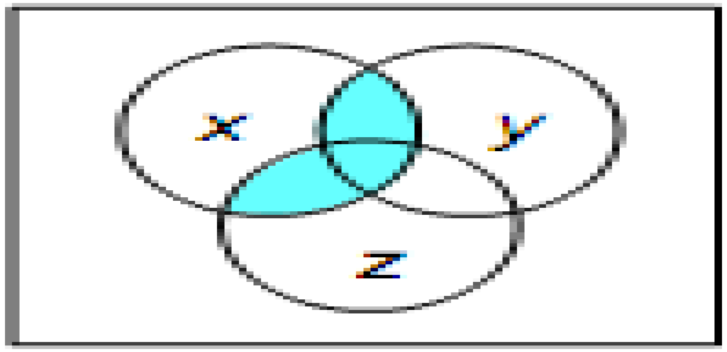
$$x \cdot (y + z) = x \cdot y + x \cdot z$$



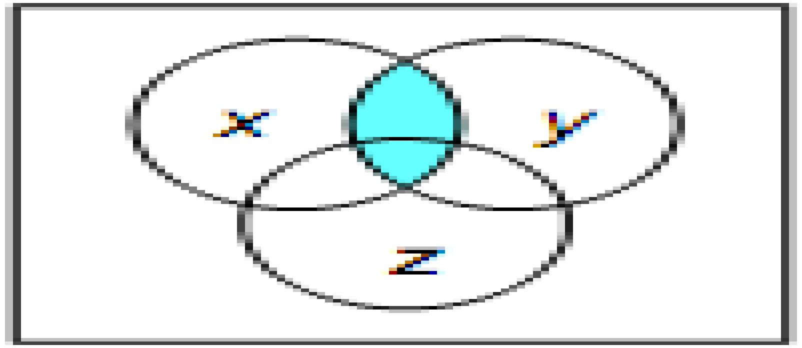
(a) x



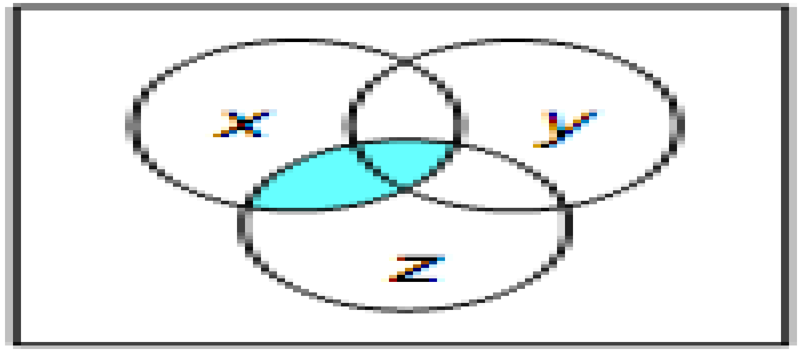
(b) $y+z$



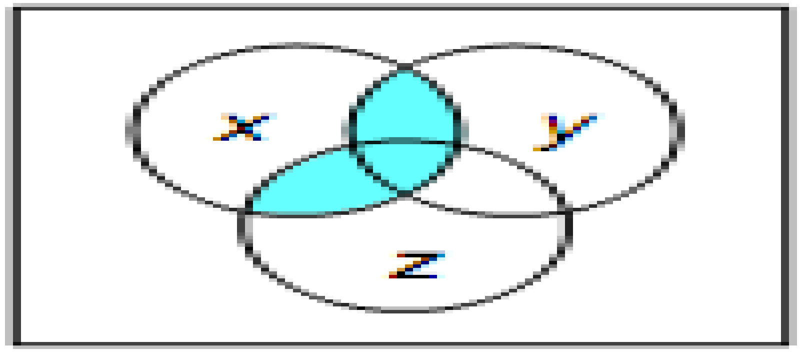
(c) $x \cdot (y+z)$



(d) $x \cdot y$

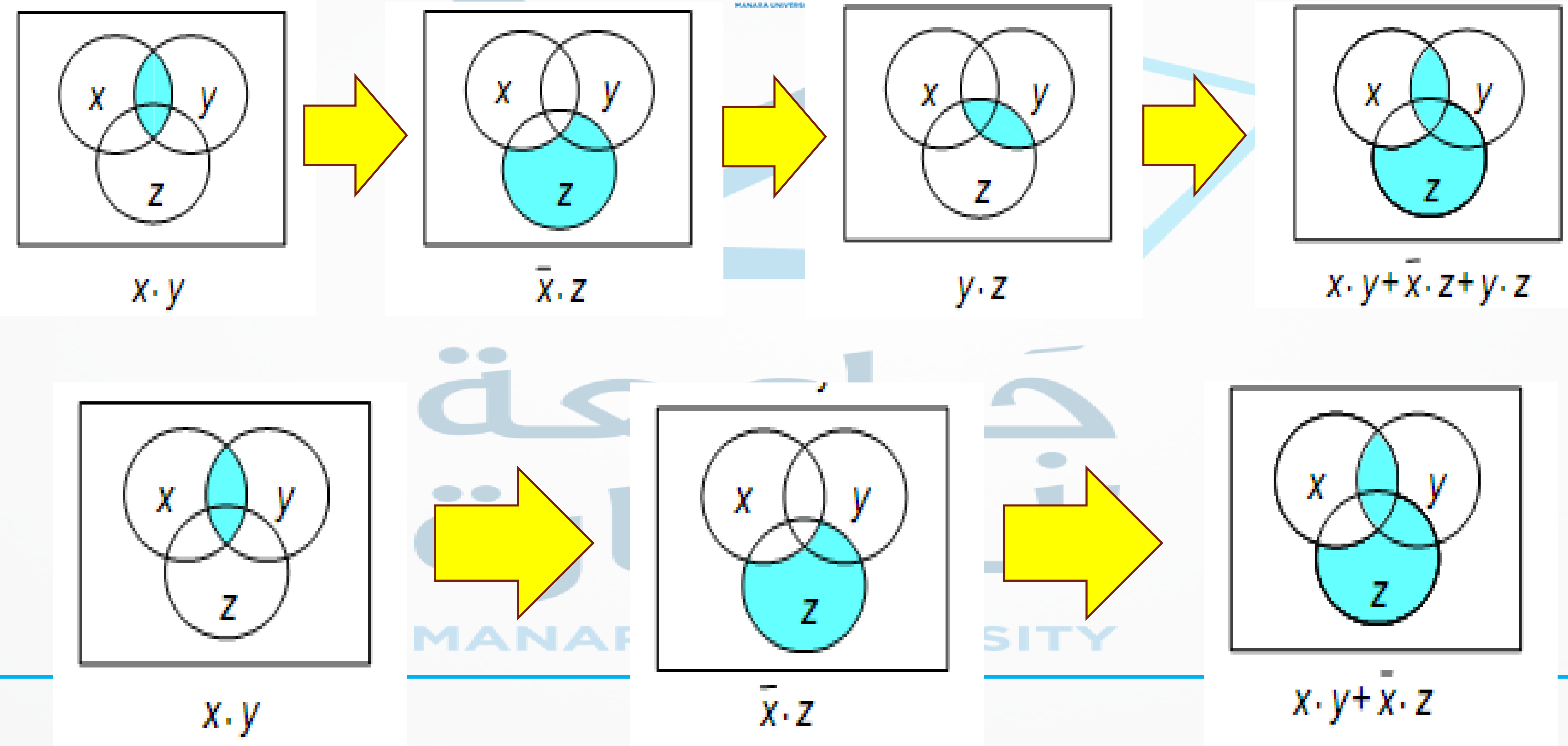


(e) $x \cdot z$



(f) $x \cdot y + x \cdot z$

Verification of $x \cdot y + \bar{x} \cdot z + y \cdot z = x \cdot y + \bar{x} \cdot z$



Synthesis of digital circuits

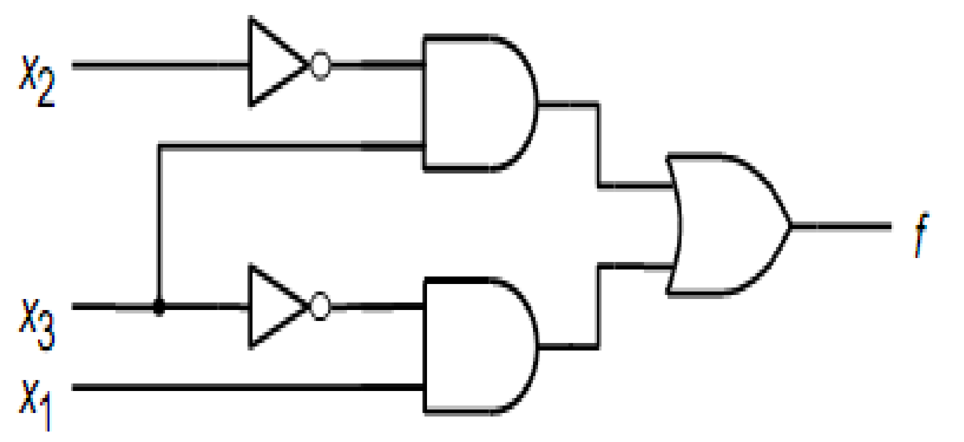
Three-variable minterms and maxterms.

Row number	x_1	x_2	x_3	Minterm	Maxterm
0	0	0	0	$m_0 = \overline{x}_1\overline{x}_2\overline{x}_3$	$M_0 = x_1 + x_2 + x_3$
1	0	0	1	$m_1 = \overline{x}_1\overline{x}_2 x_3$	$M_1 = x_1 + x_2 + \overline{x}_3$
2	0	1	0	$m_2 = \overline{x}_1 x_2\overline{x}_3$	$M_2 = x_1 + \overline{x}_2 + x_3$
3	0	1	1	$m_3 = \overline{x}_1 x_2 x_3$	$M_3 = x_1 + \overline{x}_2 + \overline{x}_3$
4	1	0	0	$m_4 = x_1\overline{x}_2\overline{x}_3$	$M_4 = \overline{x}_1 + x_2 + x_3$
5	1	0	1	$m_5 = x_1\overline{x}_2 x_3$	$M_5 = \overline{x}_1 + x_2 + \overline{x}_3$
6	1	1	0	$m_6 = x_1 x_2\overline{x}_3$	$M_6 = \overline{x}_1 + \overline{x}_2 + x_3$
7	1	1	1	$m_7 = x_1 x_2 x_3$	$M_7 = \overline{x}_1 + \overline{x}_2 + \overline{x}_3$

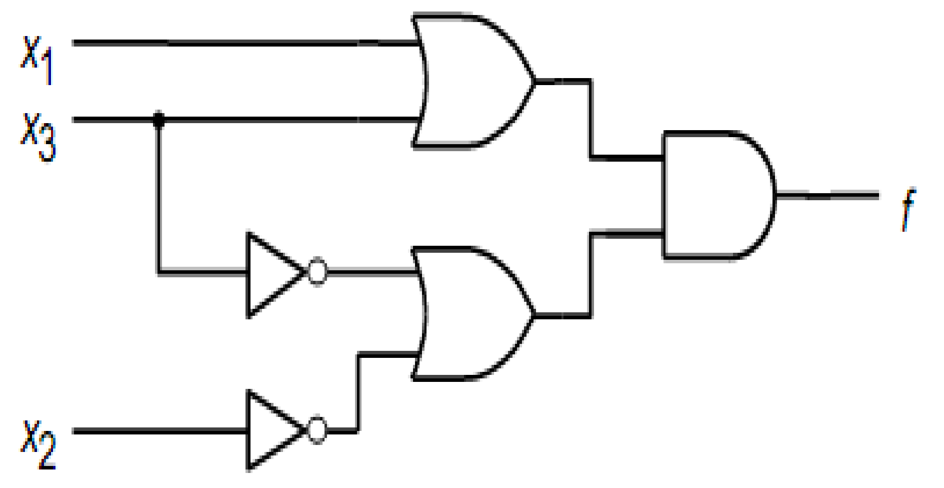
Example:

For the three variable function given by the truth table, determine the minterms, maxterms, canonical SOP, canonical POS, minterm list.

x_1	x_2	x_3	f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

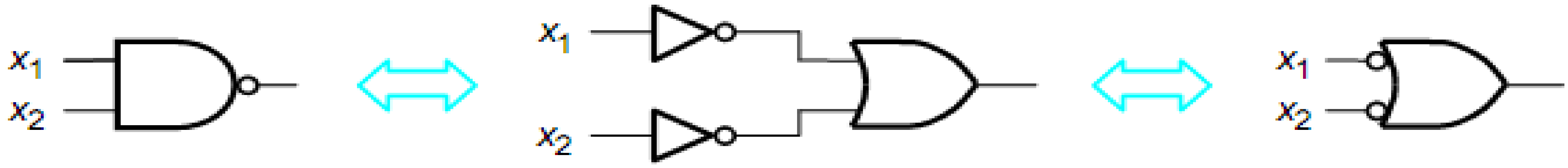


Sum-of-products realization

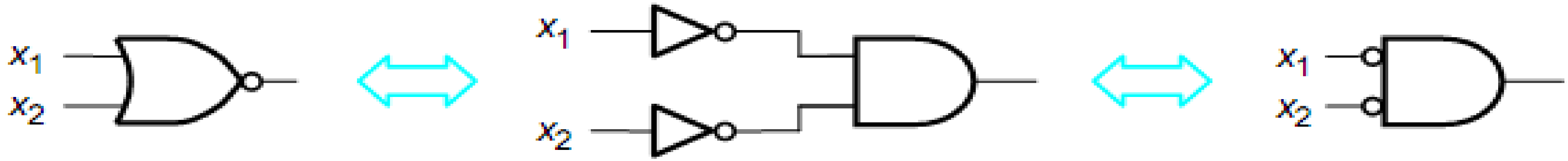


Product-of-sums realizations

DeMorgan's equivalents of NAND and NOR gates.

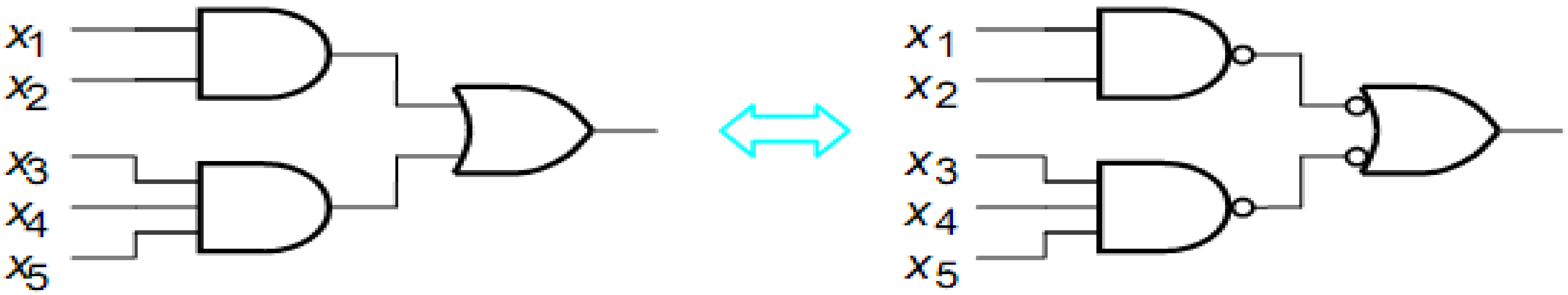


(a) $\overline{x_1 x_2} = \bar{x}_1 + \bar{x}_2$

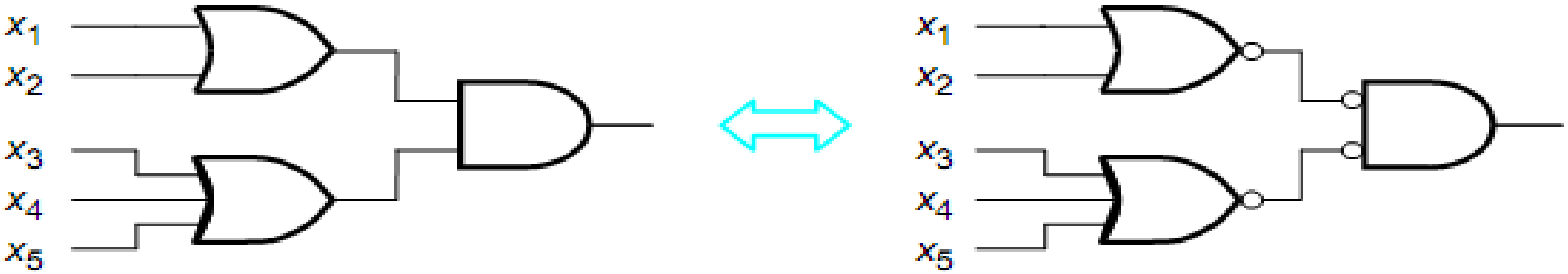


(b) $\overline{x_1 + x_2} = \bar{x}_1 \bar{x}_2$

- Converting a AND-OR realization of an SOP to a NAND-NAND realization



- Converting a OR-AND realization of a POS to a NOR-NOR realization



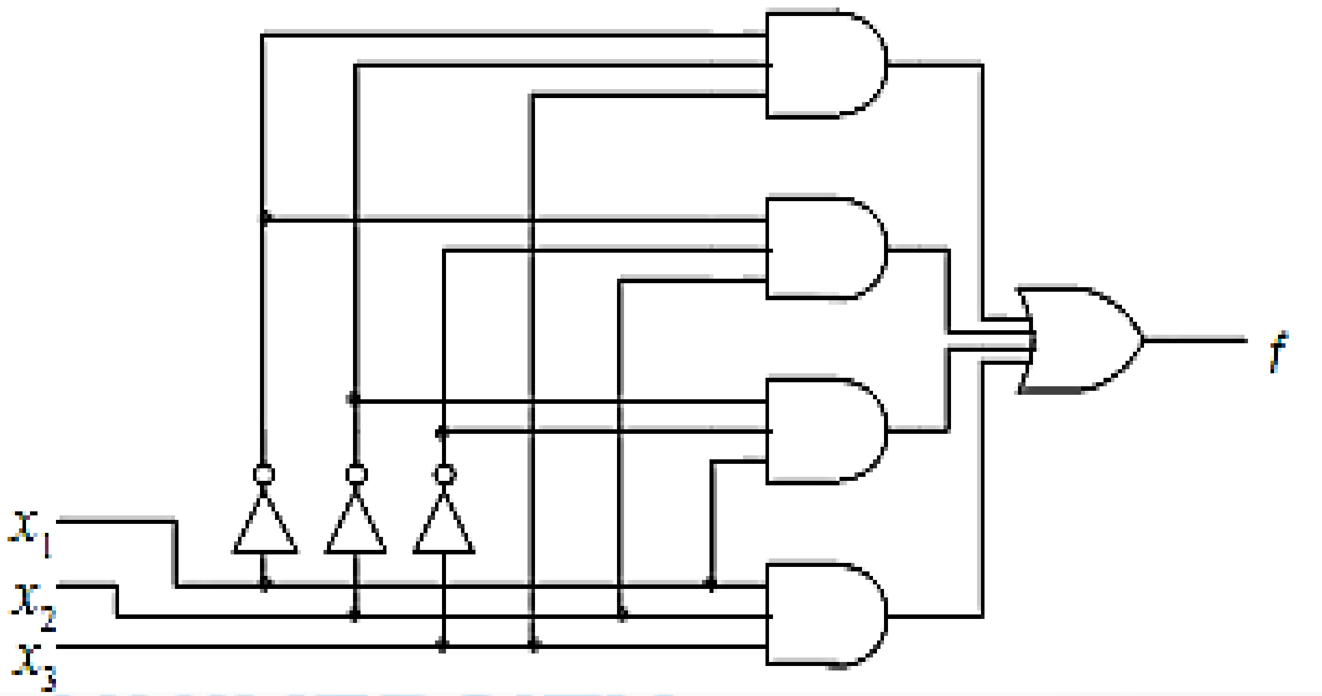
realization of an SOP

$$f(x_1, x_2, x_3) = \sum m(1, 2, 4, 7)$$

$$= (\overline{x_1}.\overline{x_2}.x_3) + (\overline{x_1}.x_2.\overline{x_3}) + (x_1.\overline{x_2}.\overline{x_3}) + (x_1.x_2.x_3)$$

x_1	x_2	x_3	f
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Sum-of-products realizations



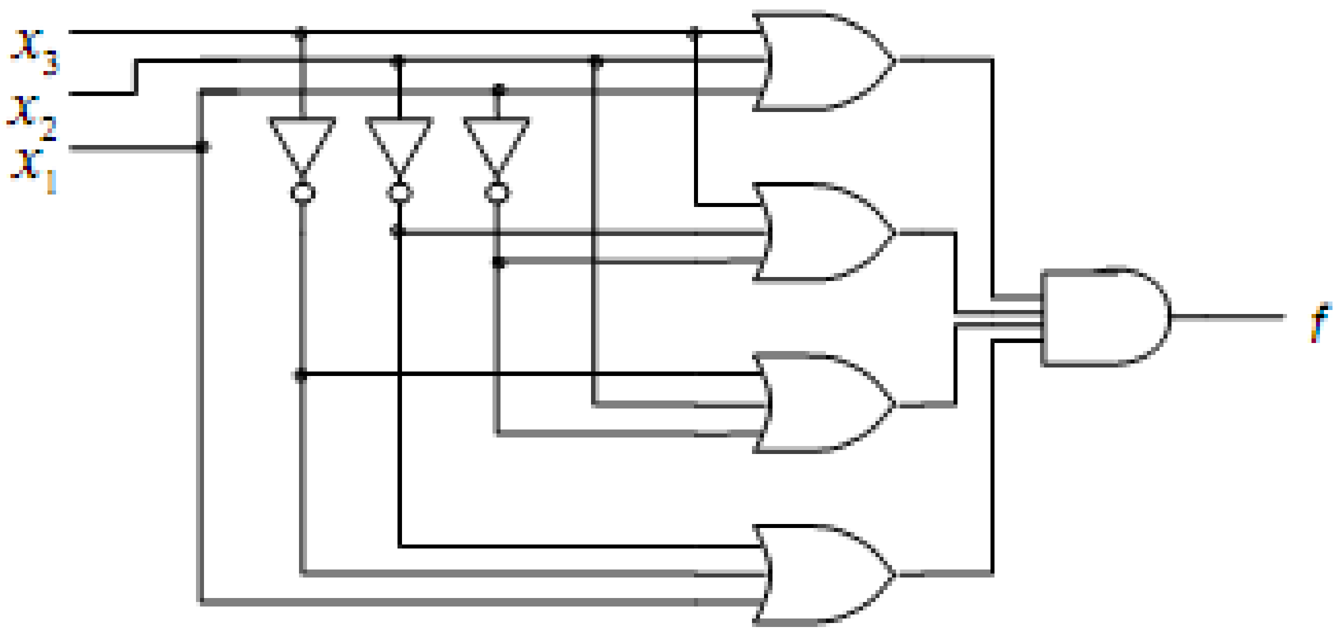
realization of an POS

x_1	x_2	x_3	f
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

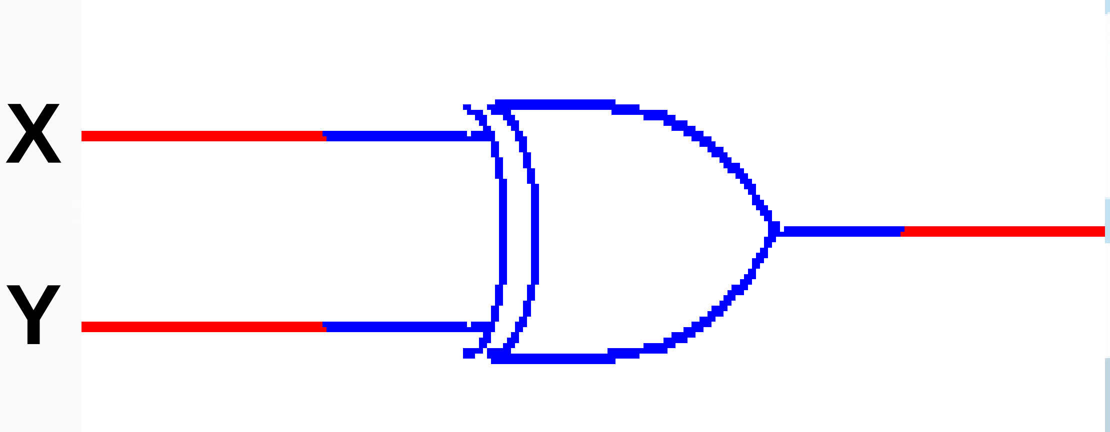
$$f(x_1, x_2, x_3) = \prod M(0, 3, 5, 6)$$

$$f(x_1, x_2, x_3) = (x_1 + x_2 + x_3)(x_1 + \overline{x_2} + \overline{x_3})(\overline{x_1} + x_2 + \overline{x_3})(x_1 + x_2 + \overline{x_3})$$

Product-of-sums realizations



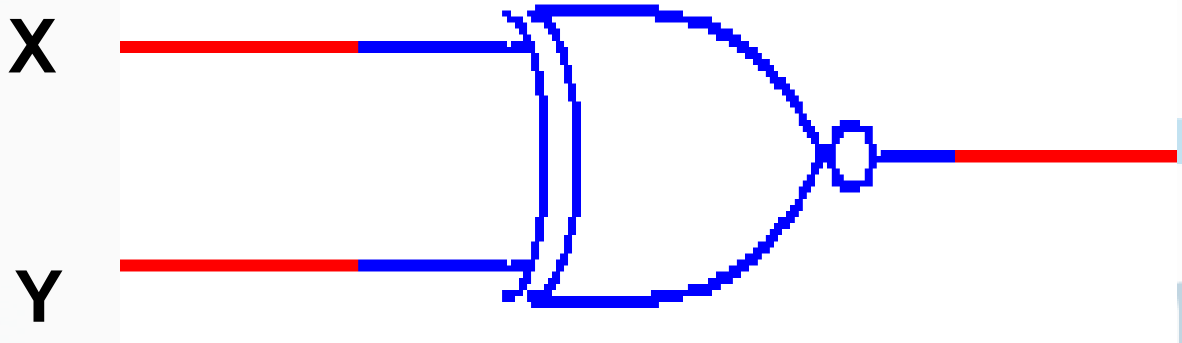
XOR Gate – Exclusive OR



$$Z = \bar{X}Y + X\bar{Y} = X \oplus Y$$

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	0

XNOR Gate – Exclusive NOR



$$Z = \overline{X}\,\overline{Y} + XY = \overline{X \oplus Y}$$

X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	1

Logic Design with XOR & XNOR

Example

Algebraically manipulate the logic expression for F_1 so that XOR and XNOR gates can be used to implement the function. Other AOI gates can be used as needed.

$$F_1 = X\overline{Y}Z + \overline{X}YZ + \overline{X}\,\overline{Y}\,\overline{Z} + X\overline{Y}Z$$

Solution

$$F_1 = X\,\overline{Y}\,Z + \overline{X}\,Y\,Z + \overline{X}\,\overline{Y}\,\overline{Z} + X\,Y\,Z = Z\left(X\,\overline{Y} + \overline{X}\,Y\right) + \overline{Y}\left(\overline{X}\,\overline{Z} + X\,Z\right)$$

$$F_1 = Z\left(X \oplus Y\right) + \overline{Y}\left(\overline{X \oplus Z}\right)$$