جَامعة
المَنارة
MANARA UNIVERSITY

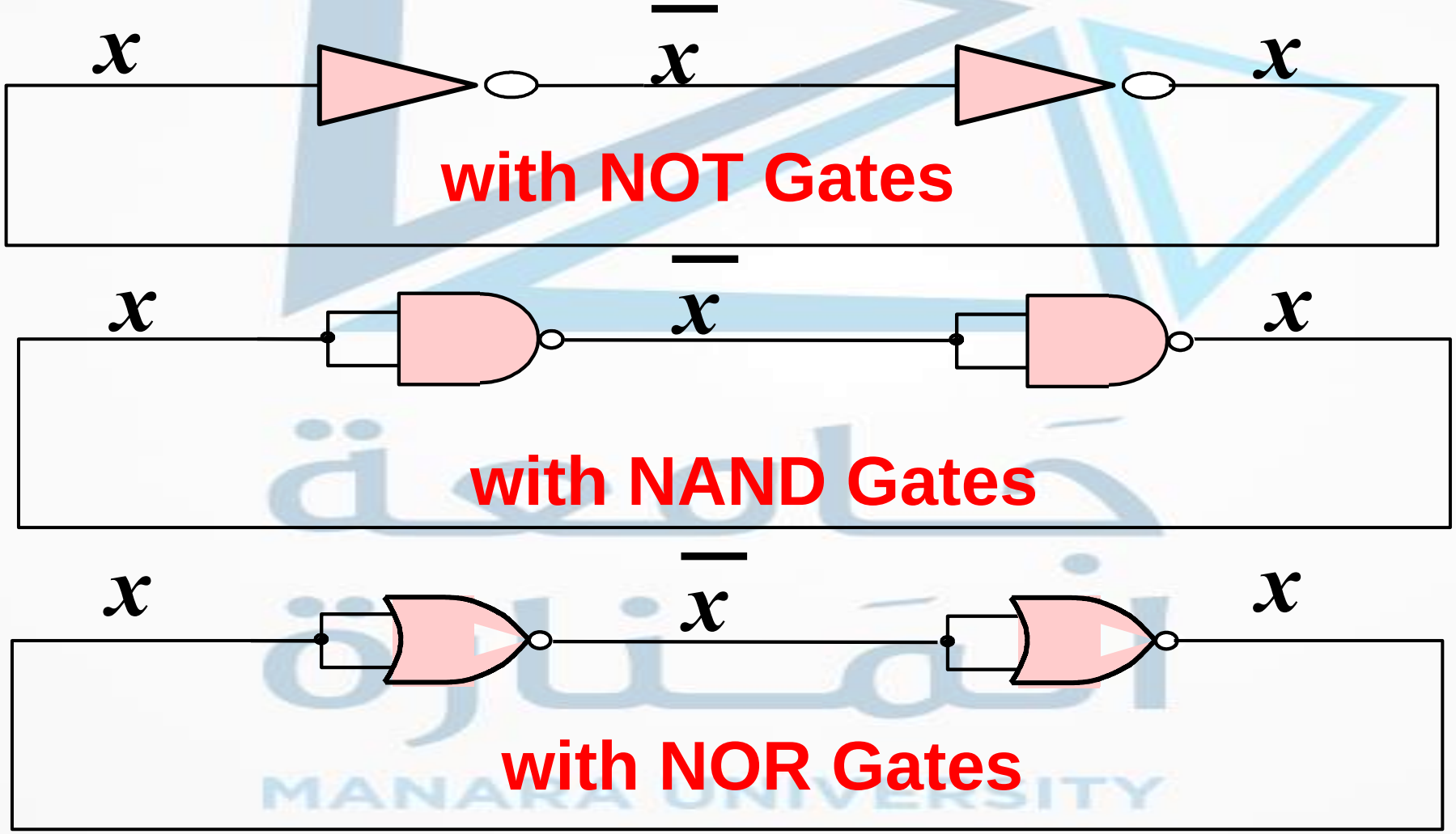
Lecture 9

OTHER COMBINATIONAL LOGIC CIRCUITS

- memory element
- Basic Latch

Dr. Bassam Atieh

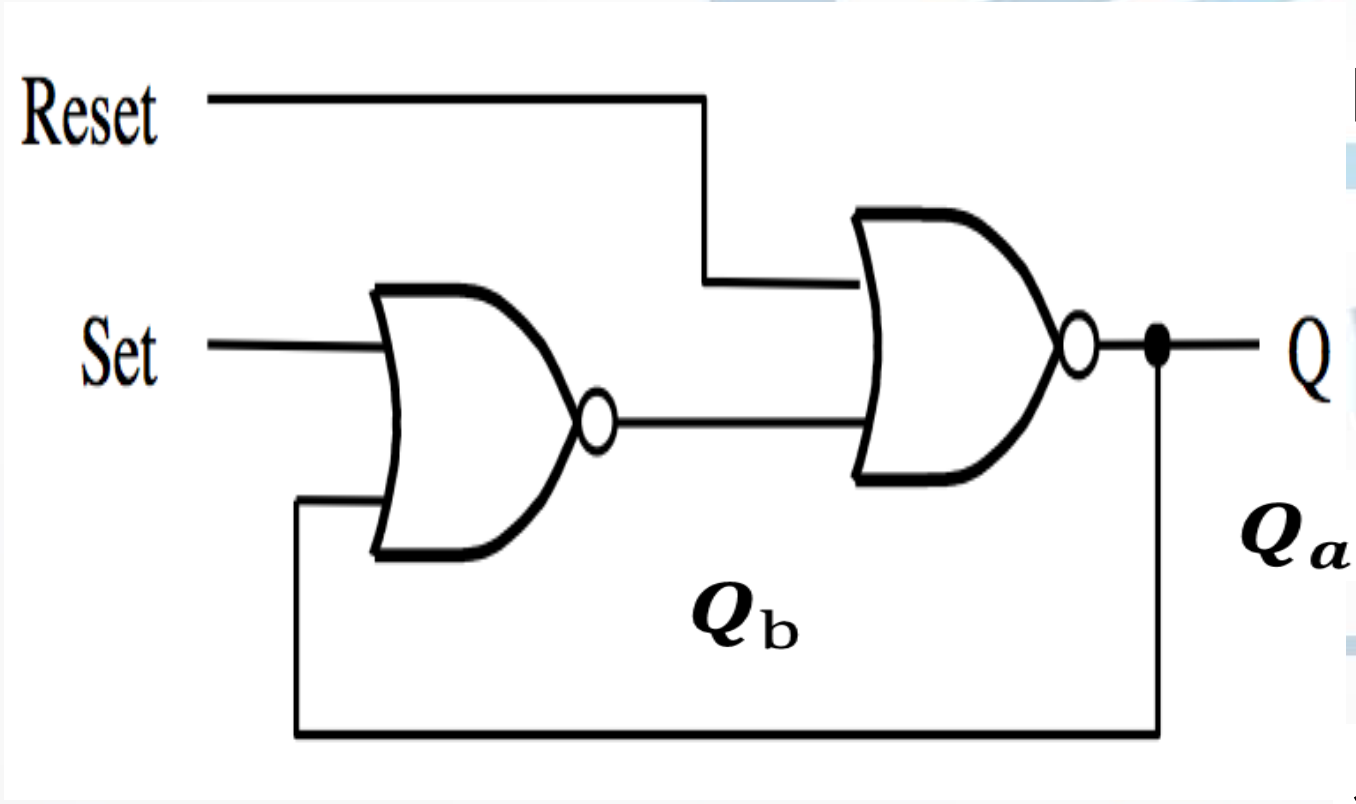
A simple memory element with NOT Gates

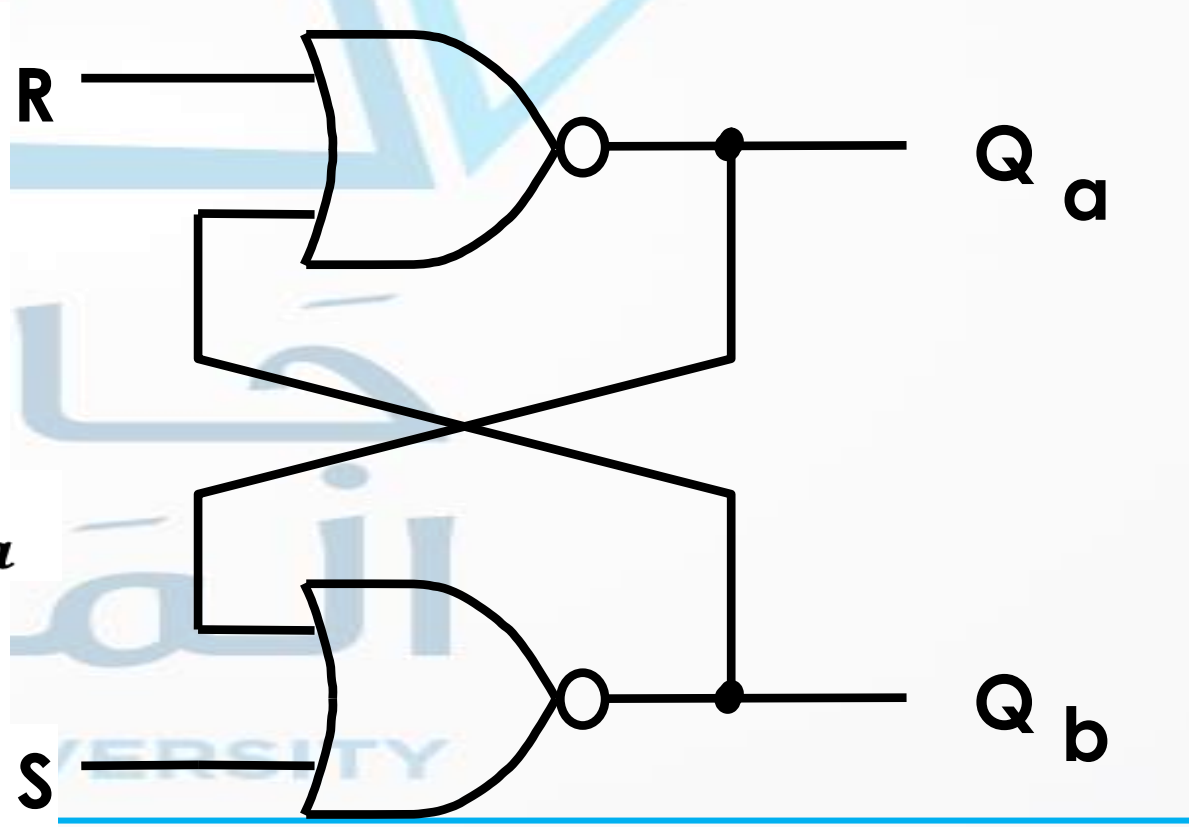


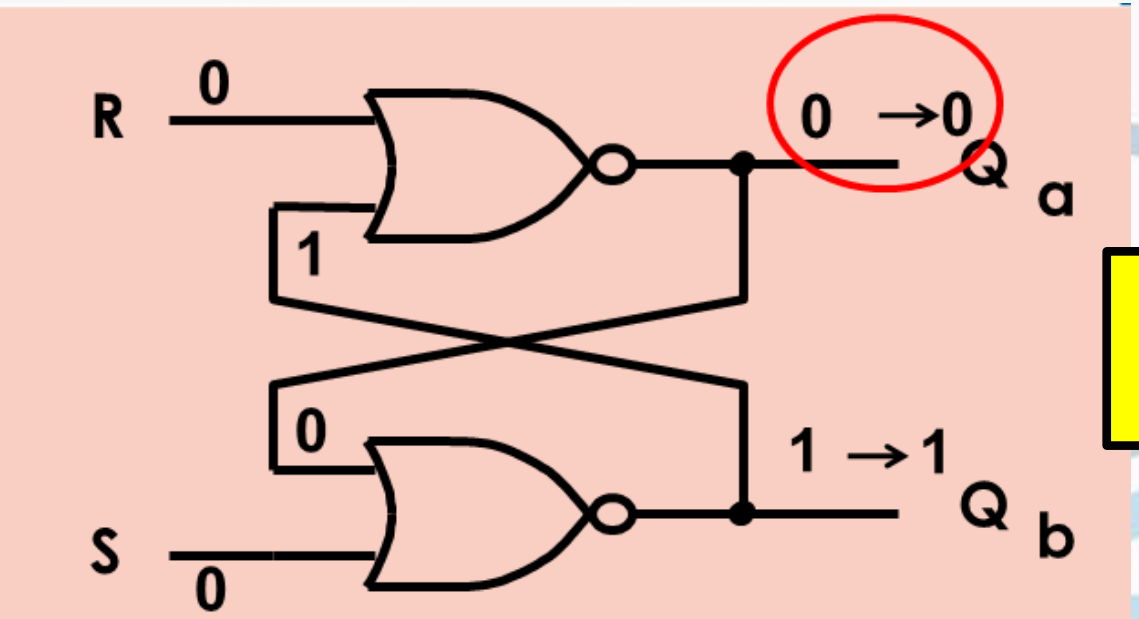
Basic Latch

Latch with NOR Gates

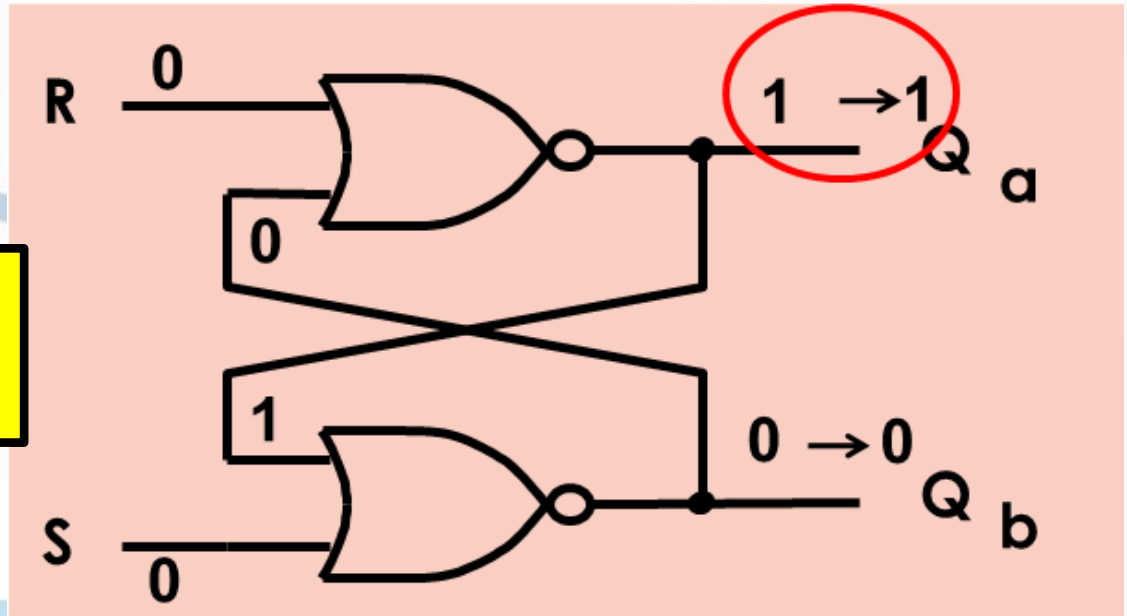
Two Different Ways to Draw the Same Circuit

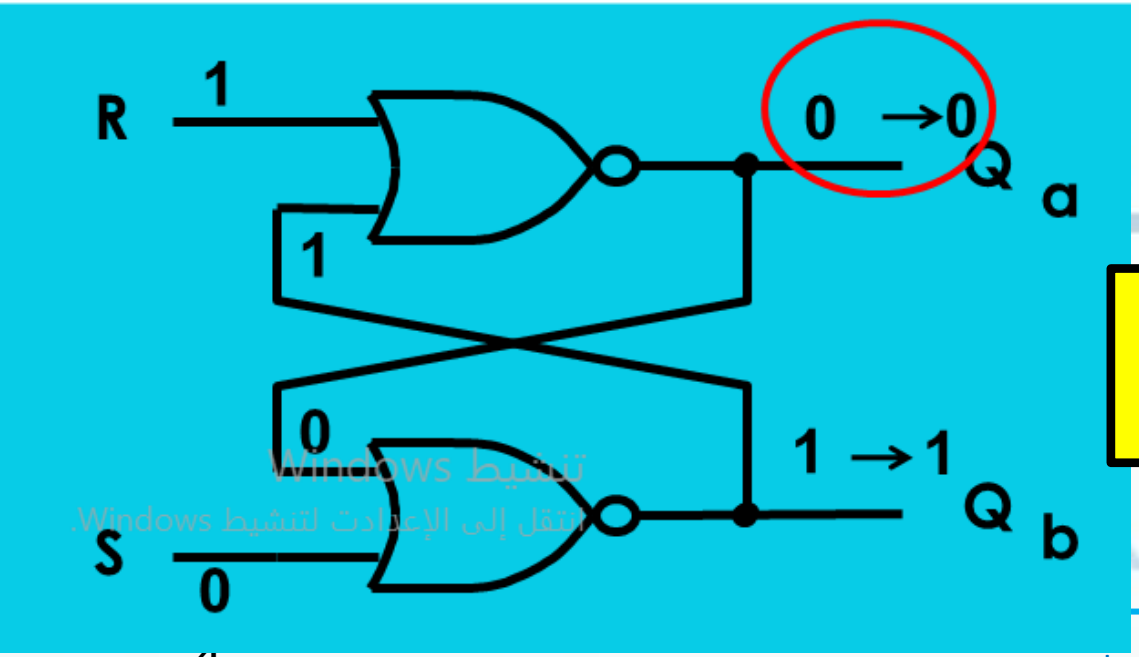




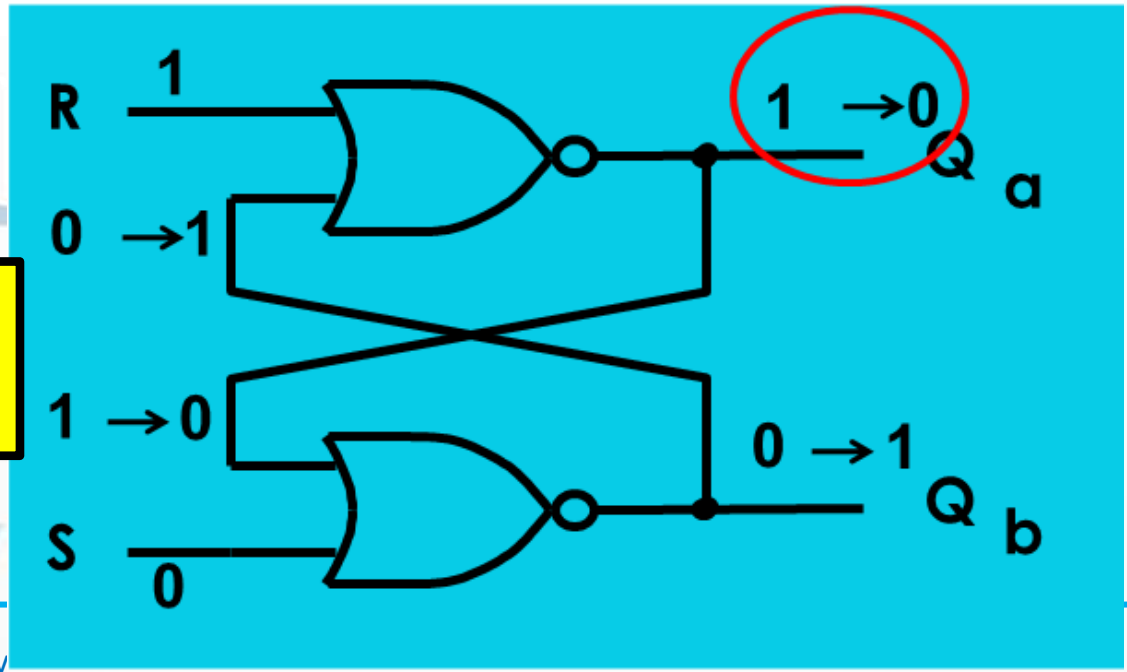


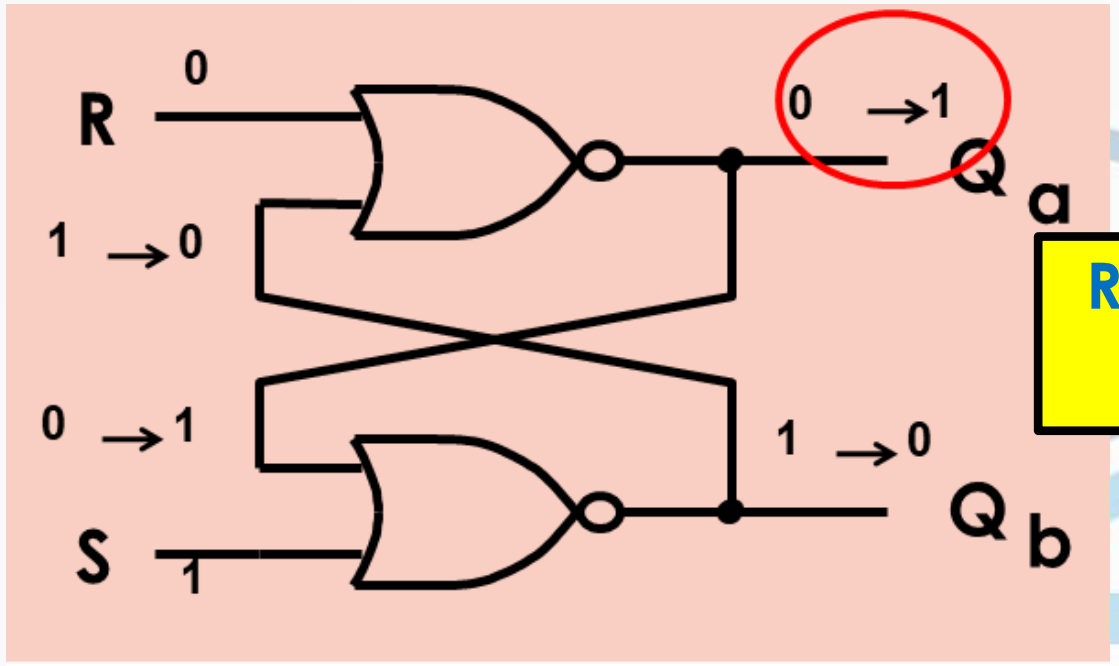
R=0 , S=0
LATCH



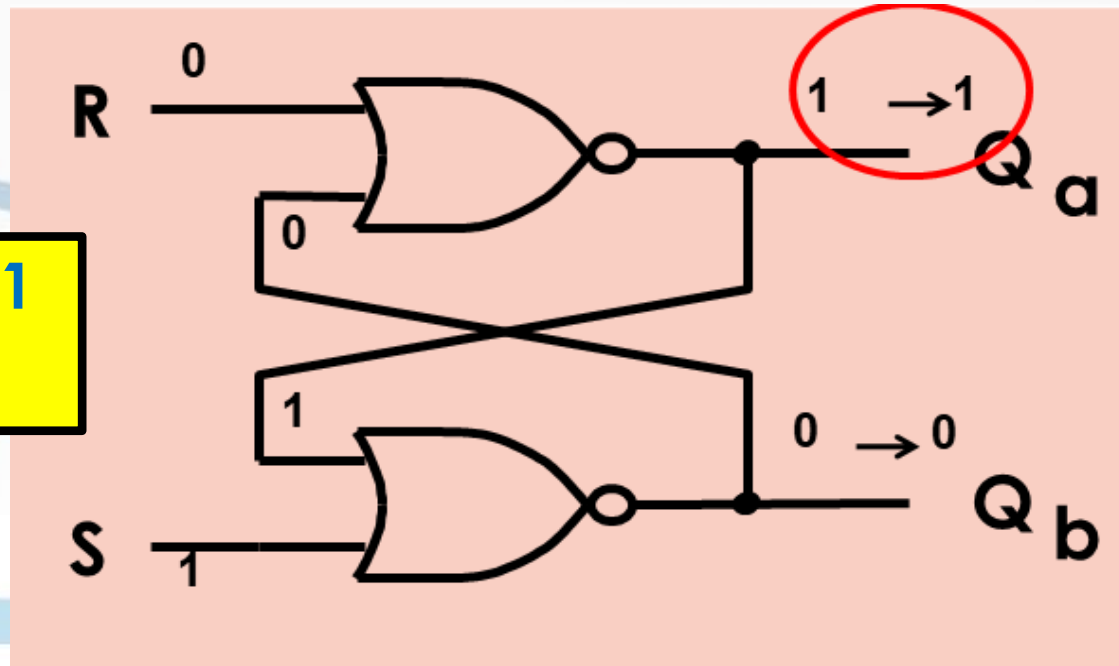


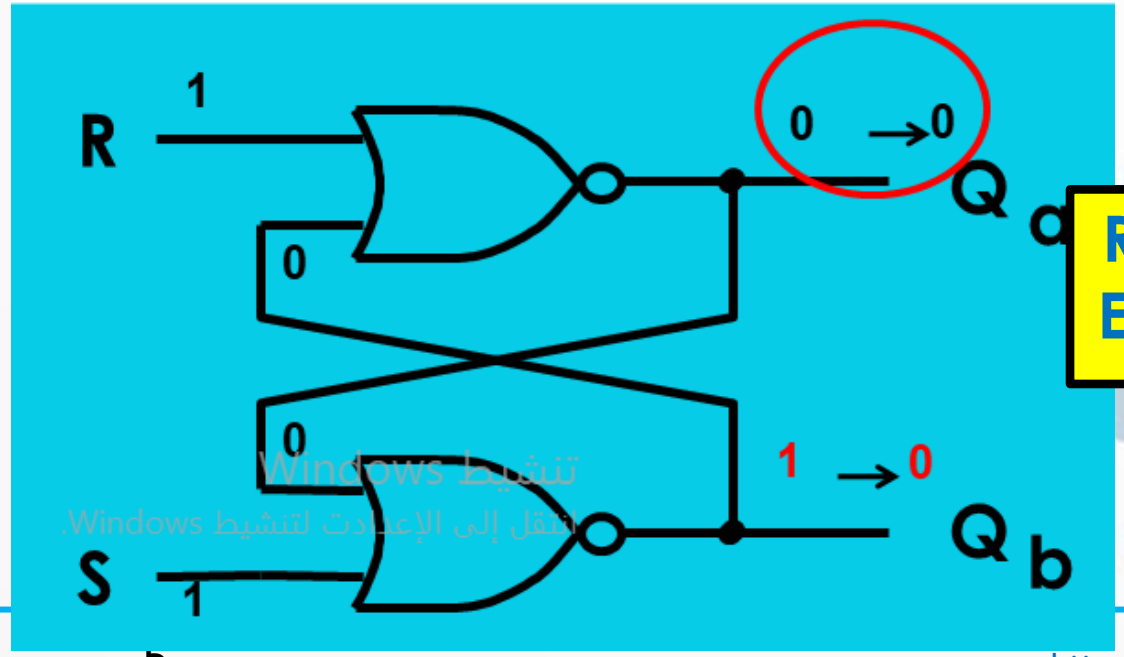
R=1 , S=0
RESET



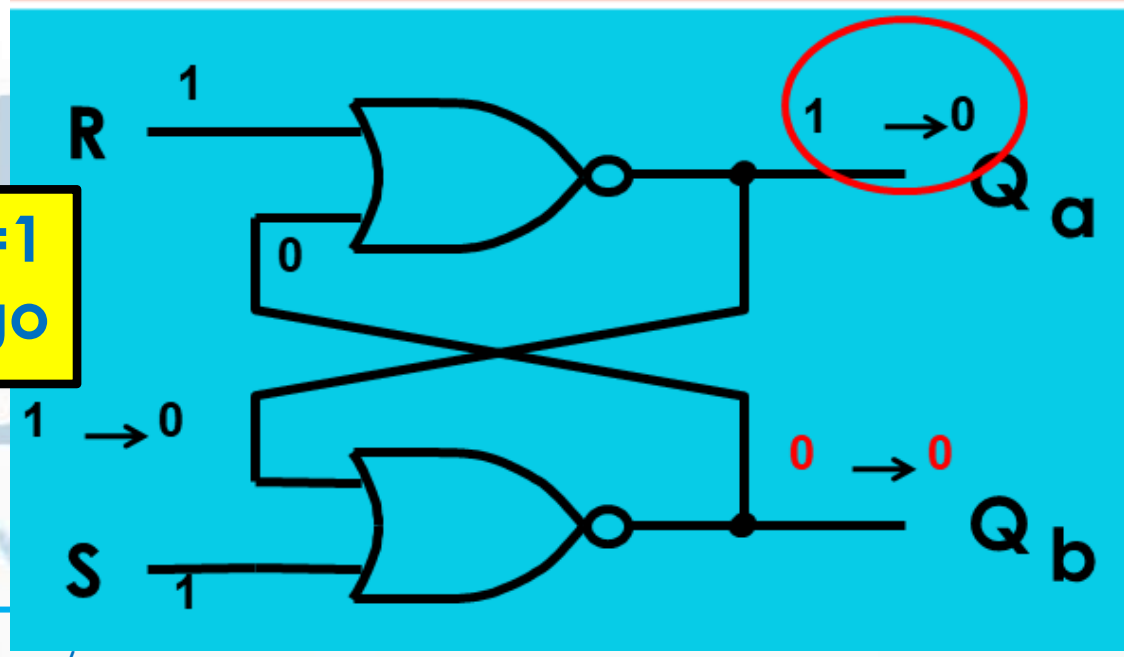


R=0 , S=1
SET





R=0 , S=1
Embargo

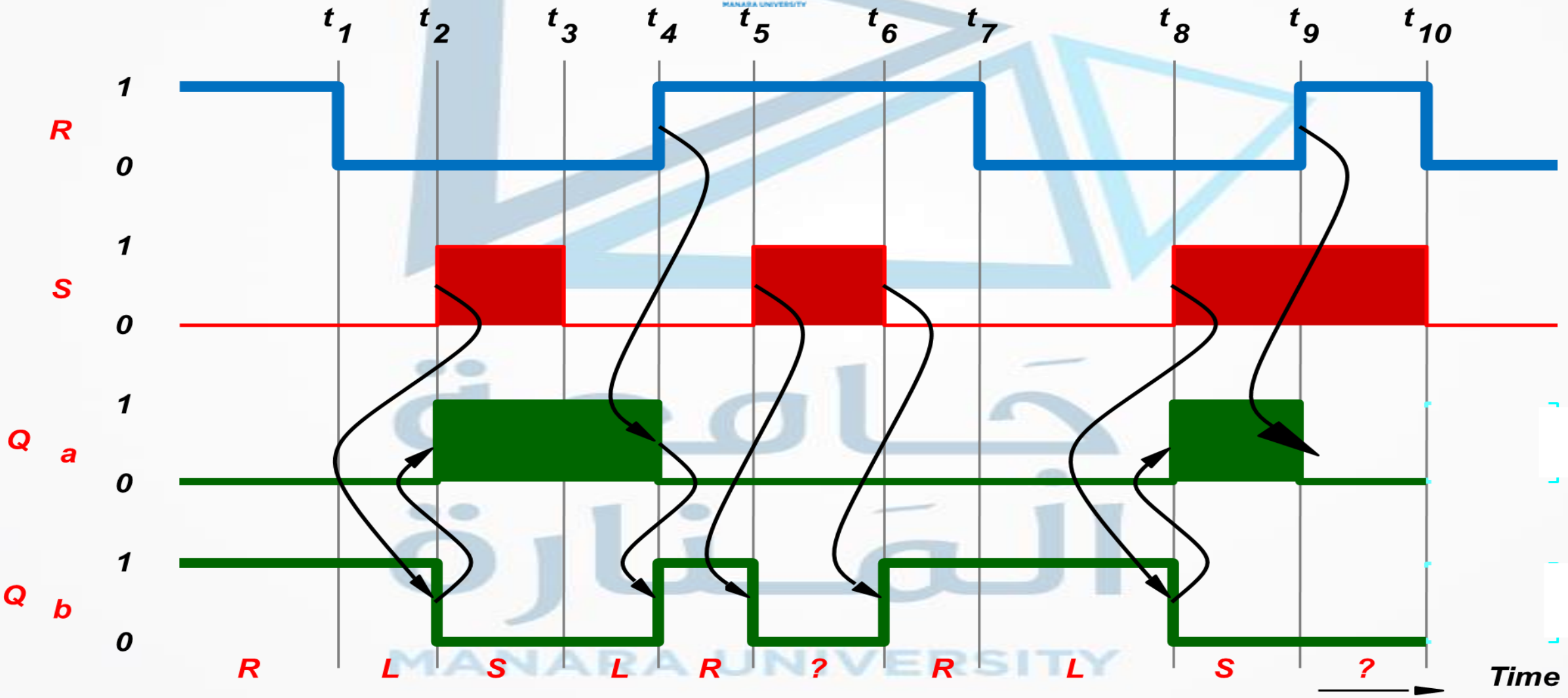


Characteristic Table
Basic Latch with NOR Gates

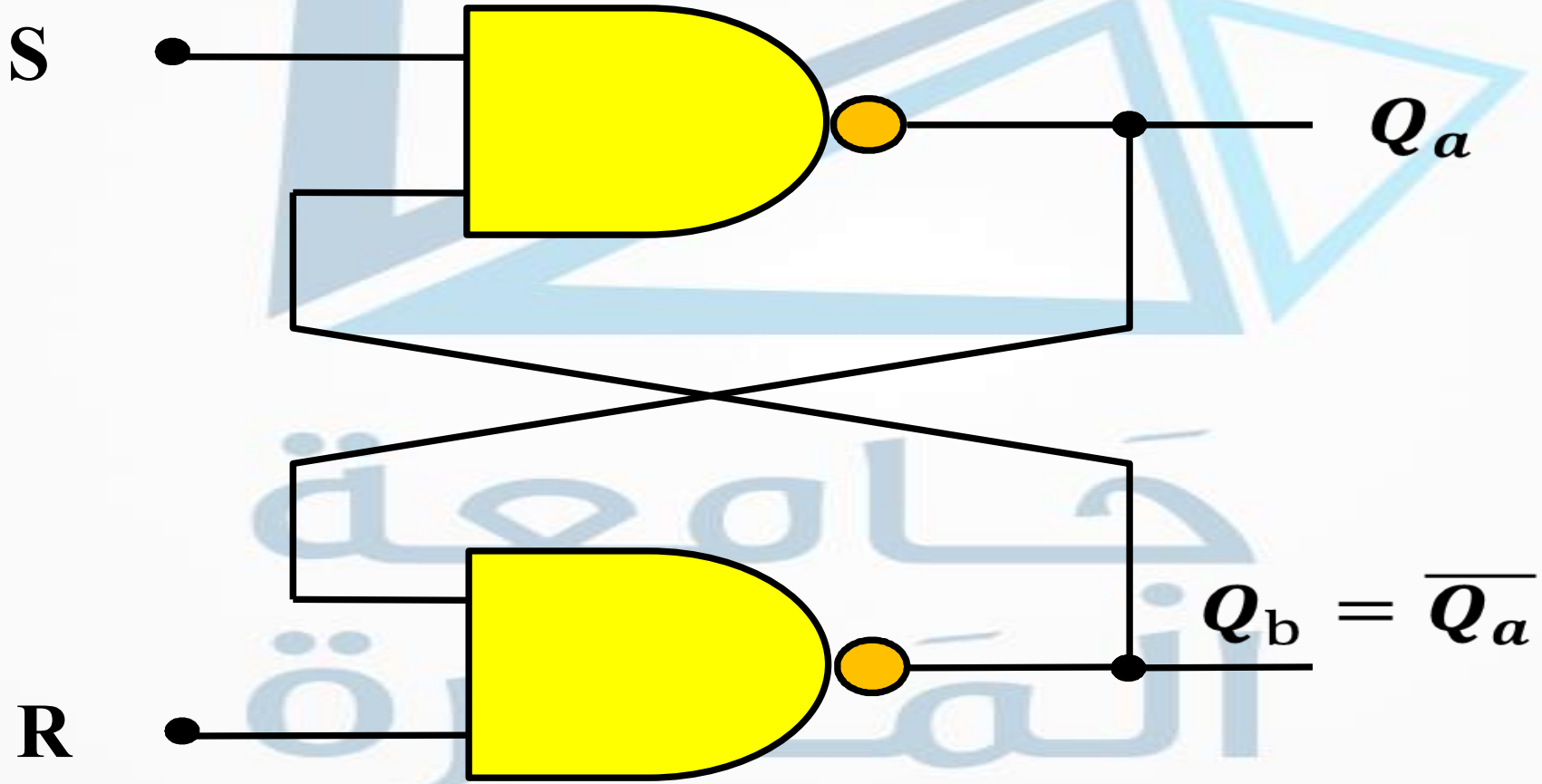
جَامعة المَنارة

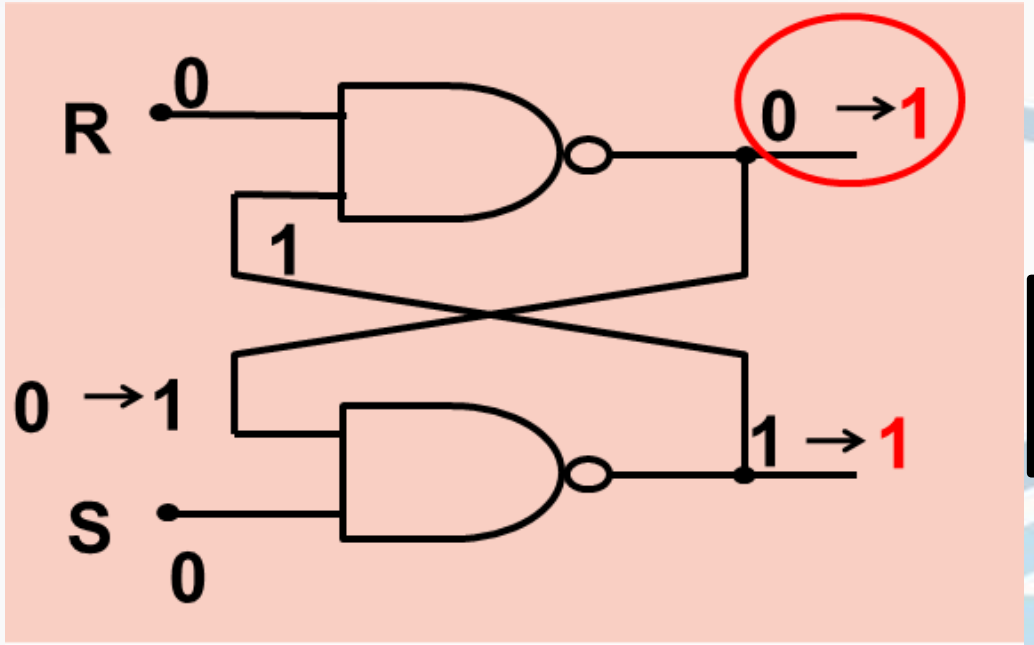
S	R	Qa-	Qa+	Qb+	state
0	0	0	0	1	R=0 S=0 LAT
0	0	1	1	0	
0	1	0	0	1	R=1 S=0 RESET
0	1	1	0	1	
1	0	0	1	0	R=0 S=1 SET
1	0	1	1	0	
1	1	0	0	0	R=1 S=1 ?
1	1	1	0	0	

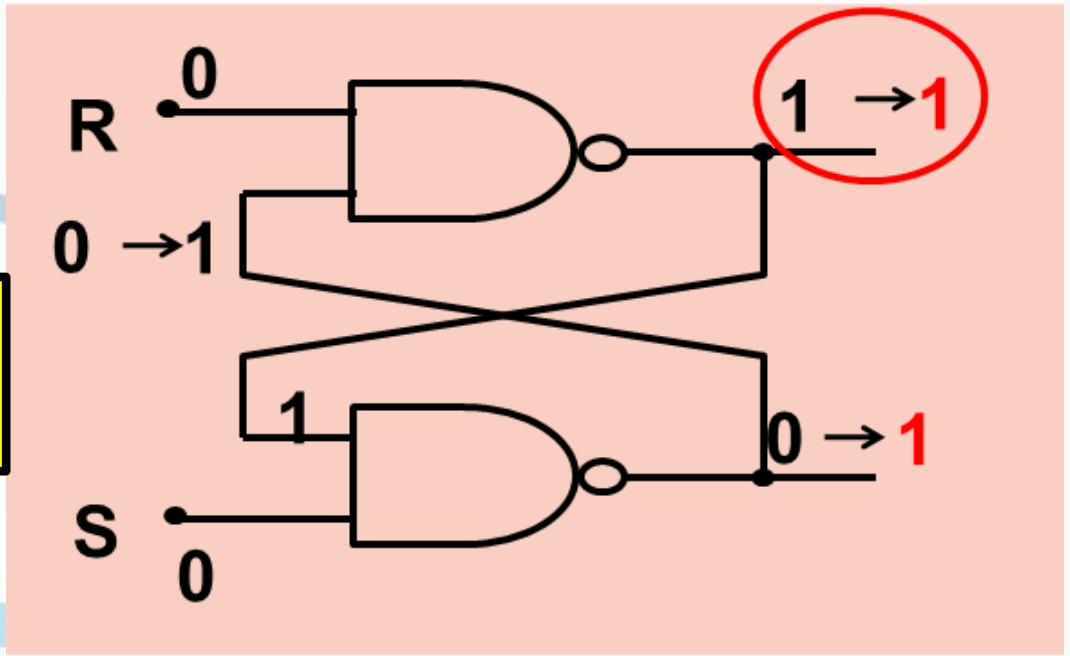
Timing Diagram for the Basic Latch with NOR Gates



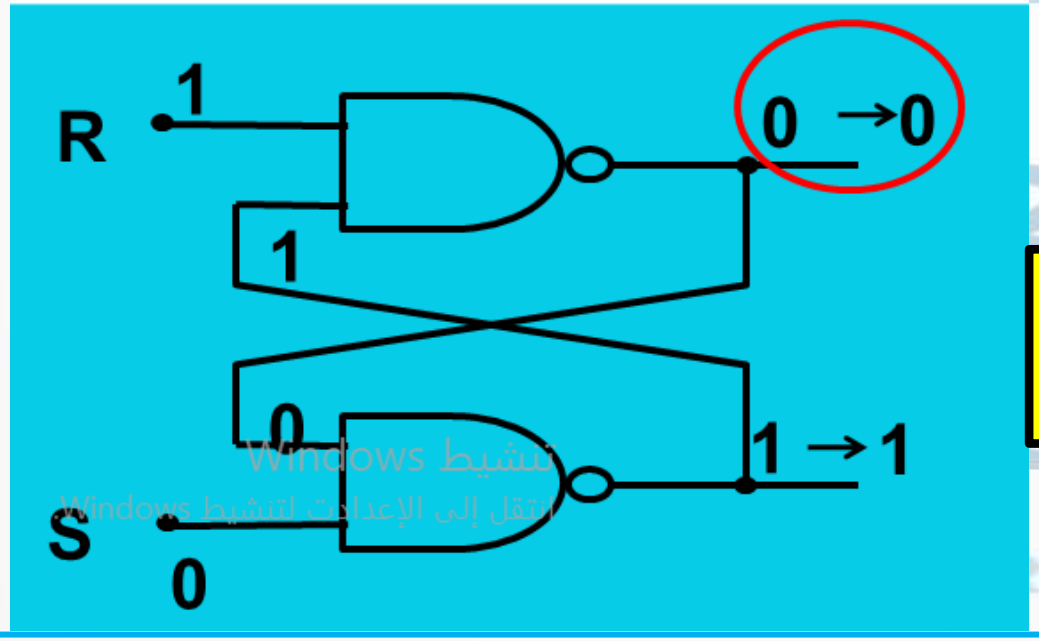
Latch with NAND Gates

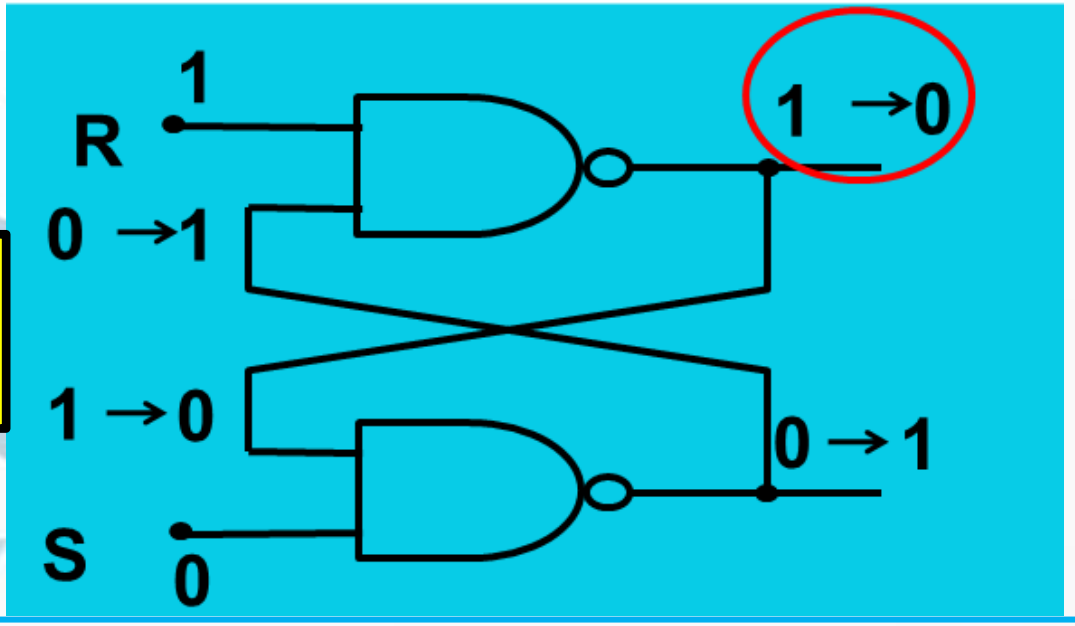




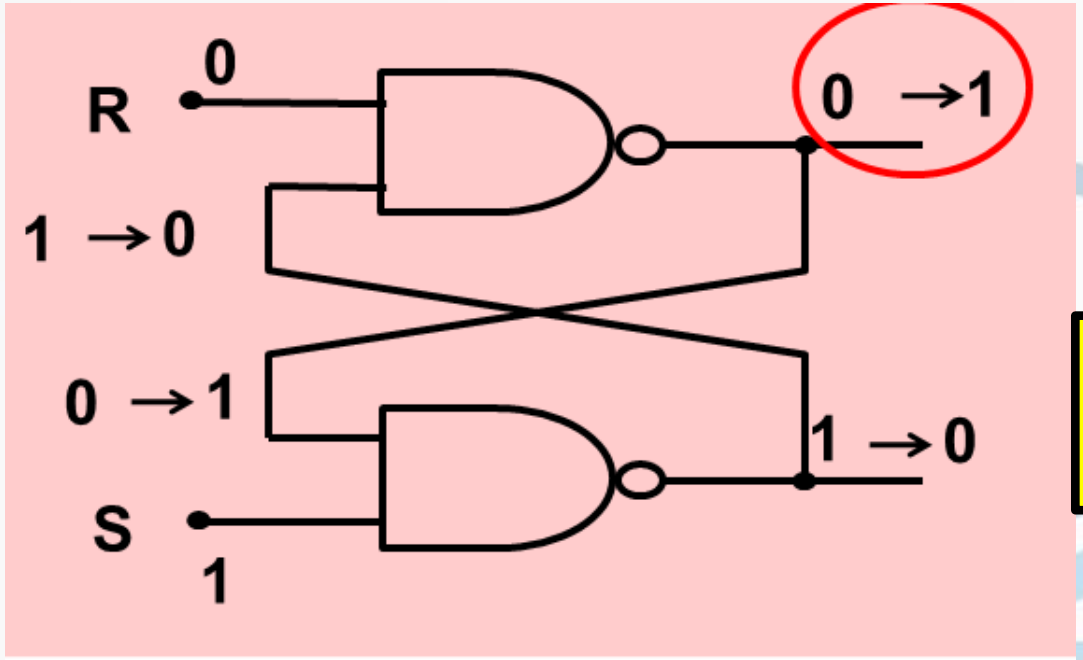


R=0 , S=0
?

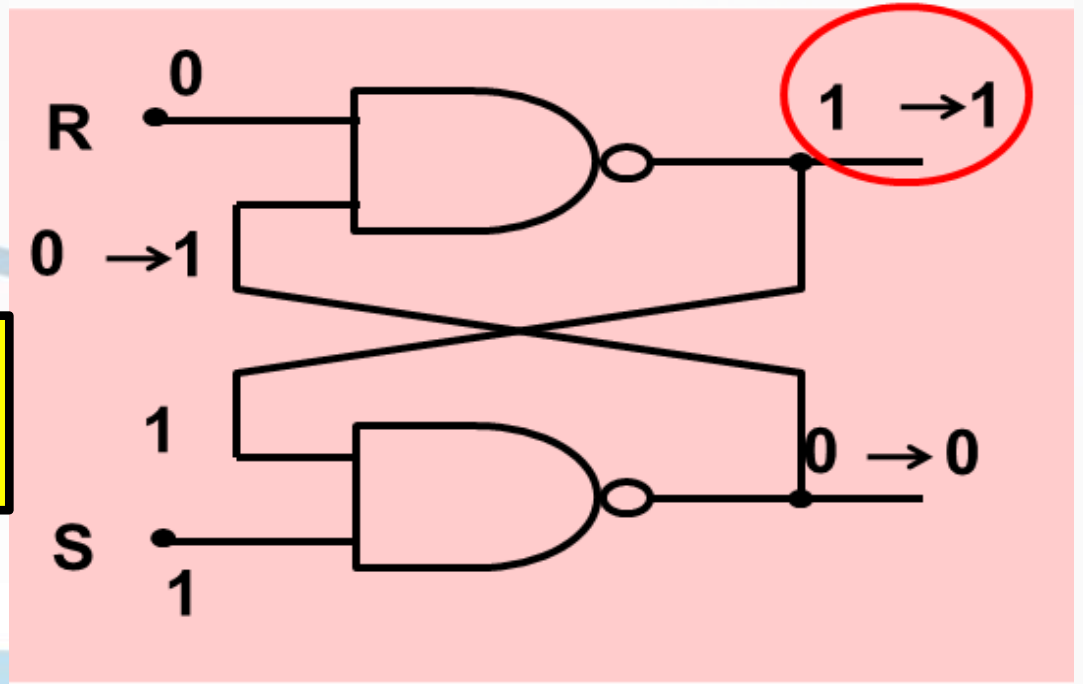


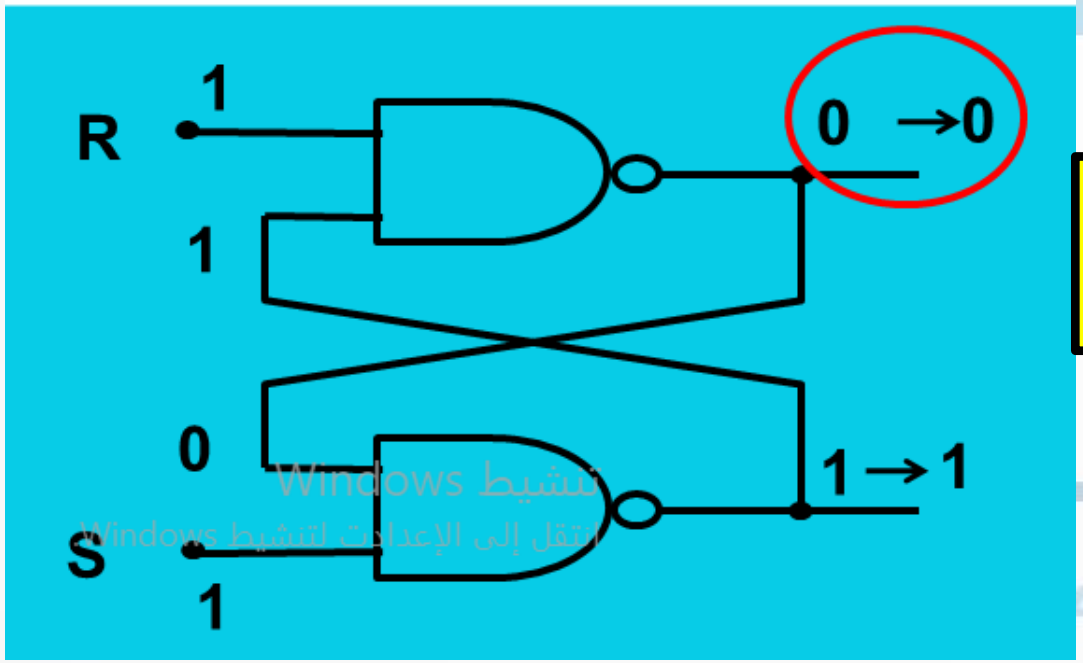


R=1 , S=0
RESET

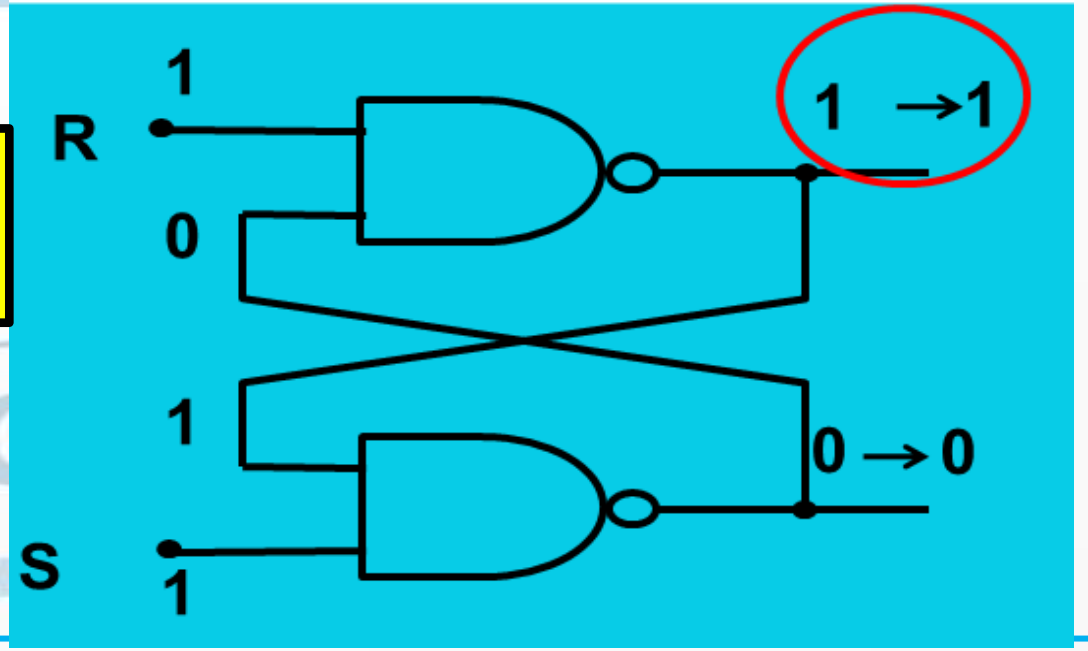


R=0 , S=1
SET





R=1 , S=1
LATCH



Characteristic Table
Basic Latch with NAND Gates

جَامعة المَنارة

S	R	Qa-	Qa+	Qb+	state
0	0	0	1	1	R=0 S=0 ?
0	0	1	1	1	
0	1	0	0	1	R=1 S=0 RESET
0	1	1	0	1	
1	0	0	1	0	R=0 S=1 SET
1	0	1	1	0	
1	1	0	0	1	R=1 S=1 LAT
1	1	1	1	0	