جَامعة
المَنارة
MANARA UNIVERSITY

Lecture 10

- Gated SR Latch

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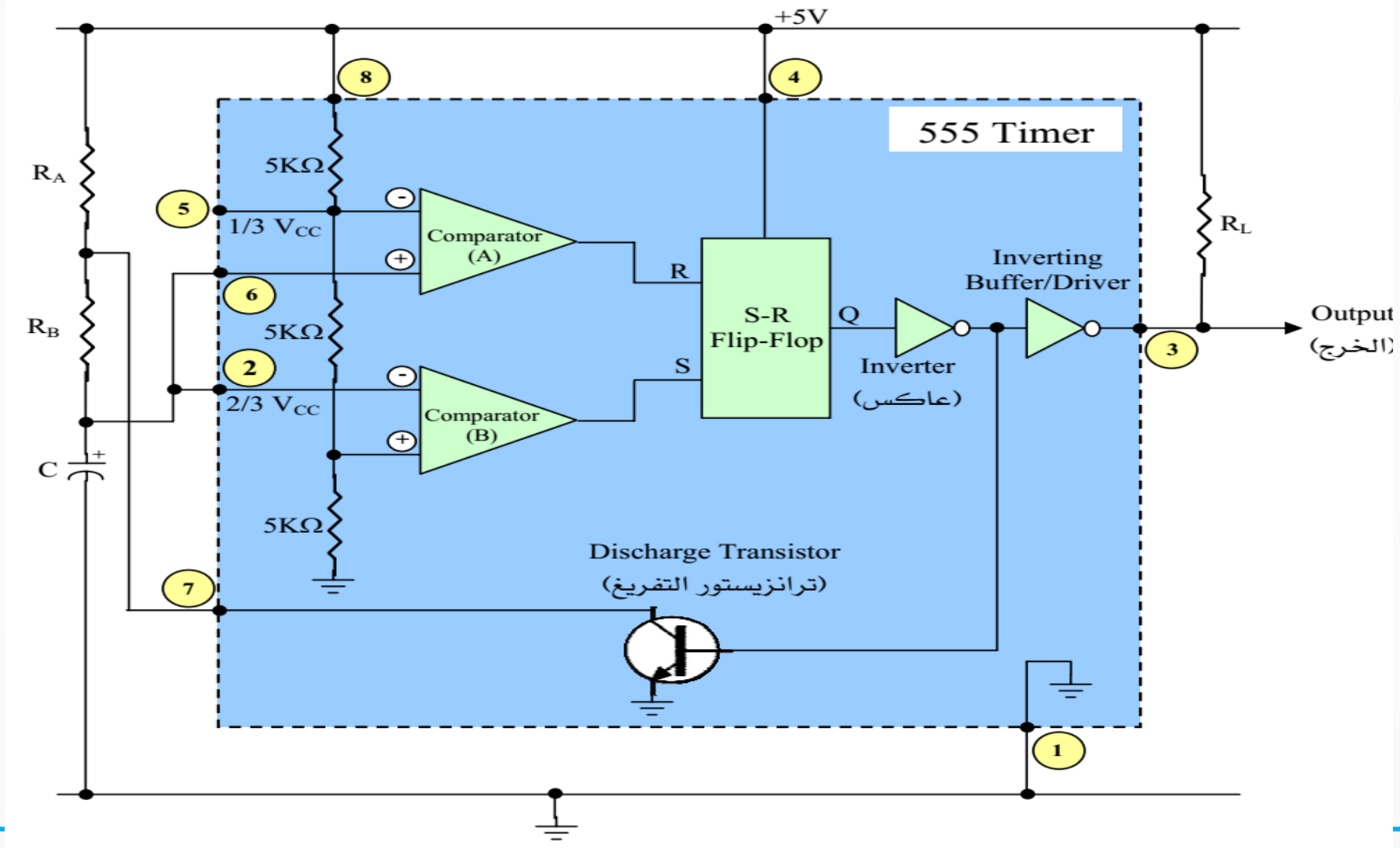
Motivation

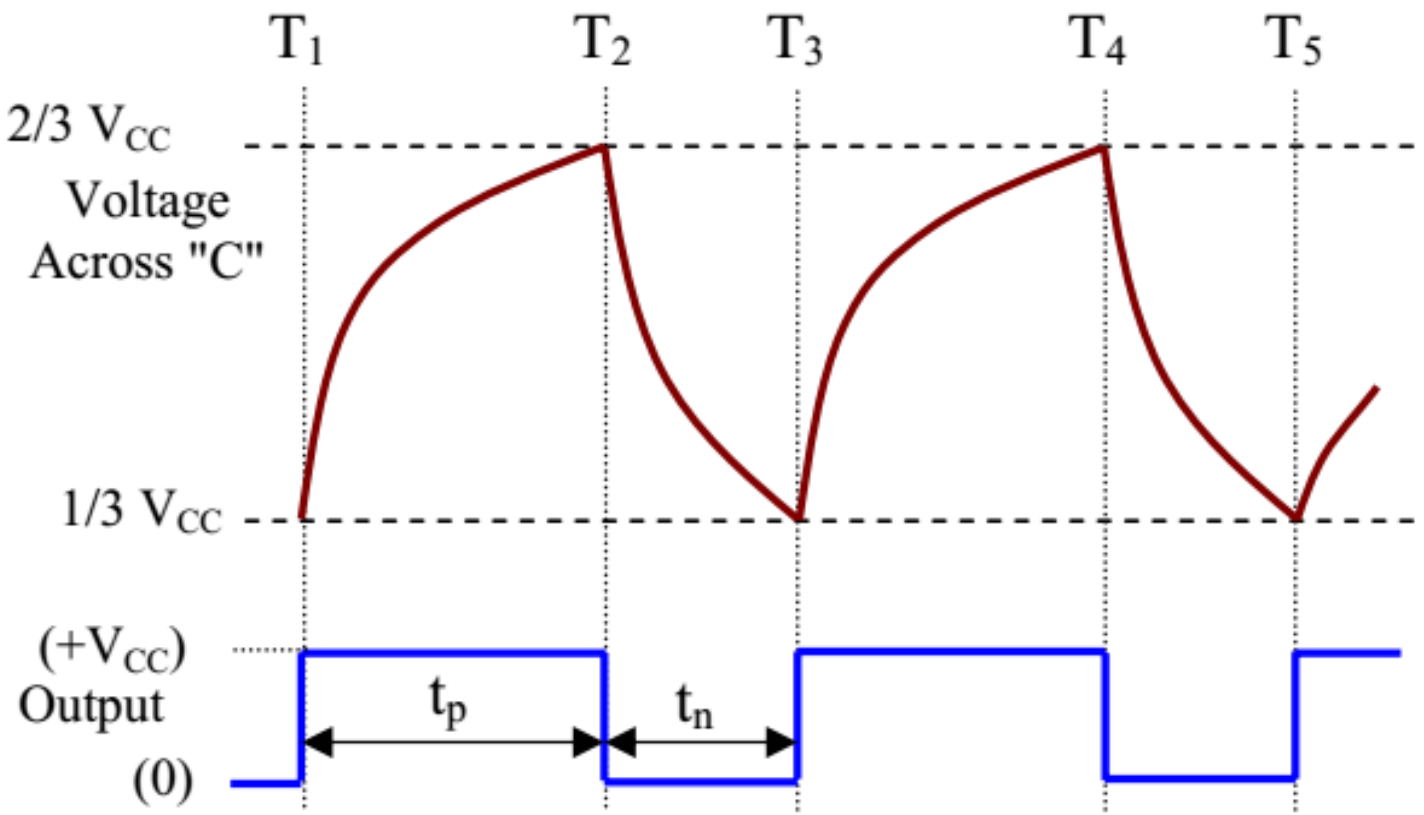
- The basic latch changes its state when the input signals change.
- It is hard to control when these input signals will change and thus it is hard to know when the latch may change its state.
- We want to have something like an Enable input.
- In this case it is called the "**Clock**" input because it is desirable for the state changes to be synchronized.

555 Timer As An stable Multivibrator

555 Timer As An stable Multivibrator Circuit



555 Timer As An stable Multivibrator Circuit



$$t_p = 0.7(R_A + R_B)C$$

$$t_n = 0.7R_BC$$

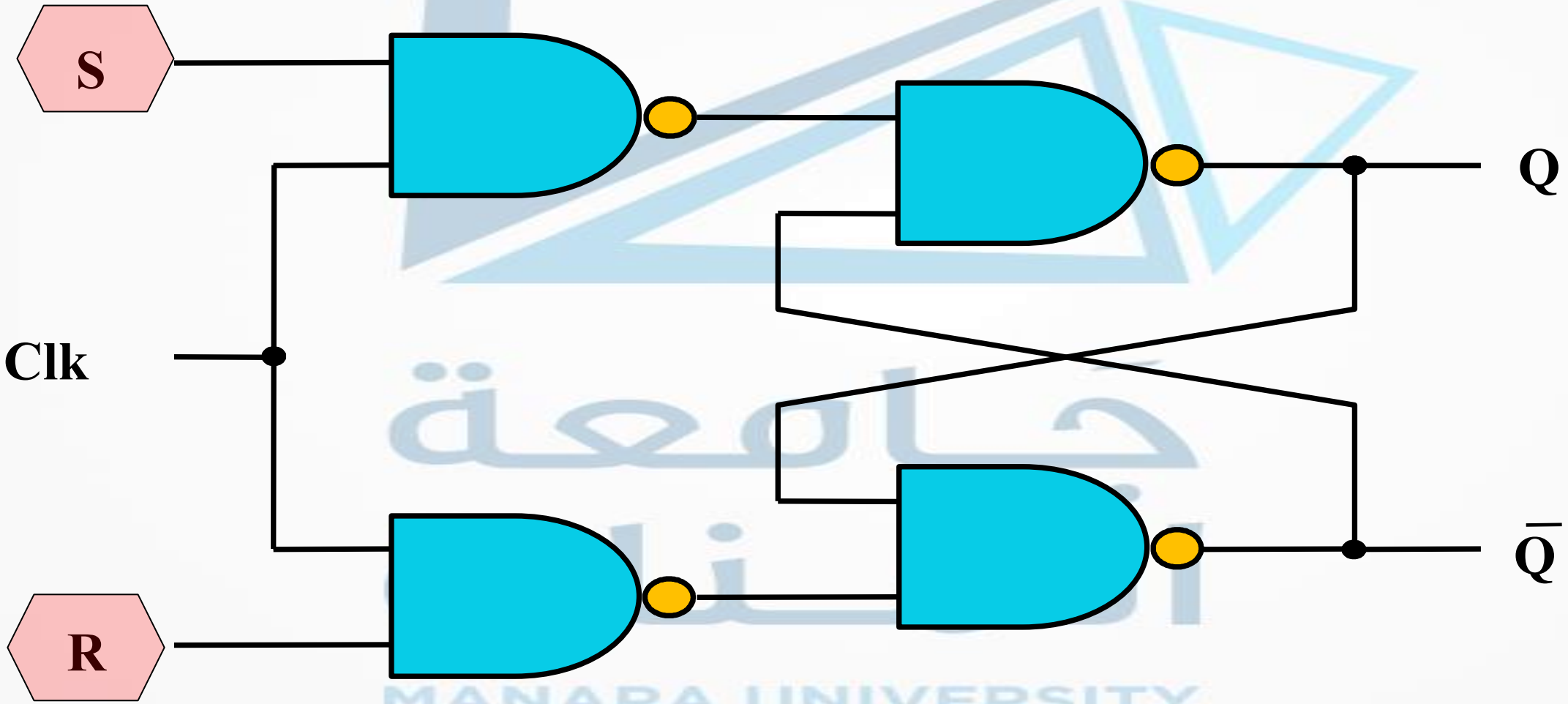
$$T = t_p + t_n$$

$$= 0.7(R_A + 2R_B)C$$

$$f = \frac{1}{T} = \frac{1}{0.7(R_A + 2R_B)C}$$

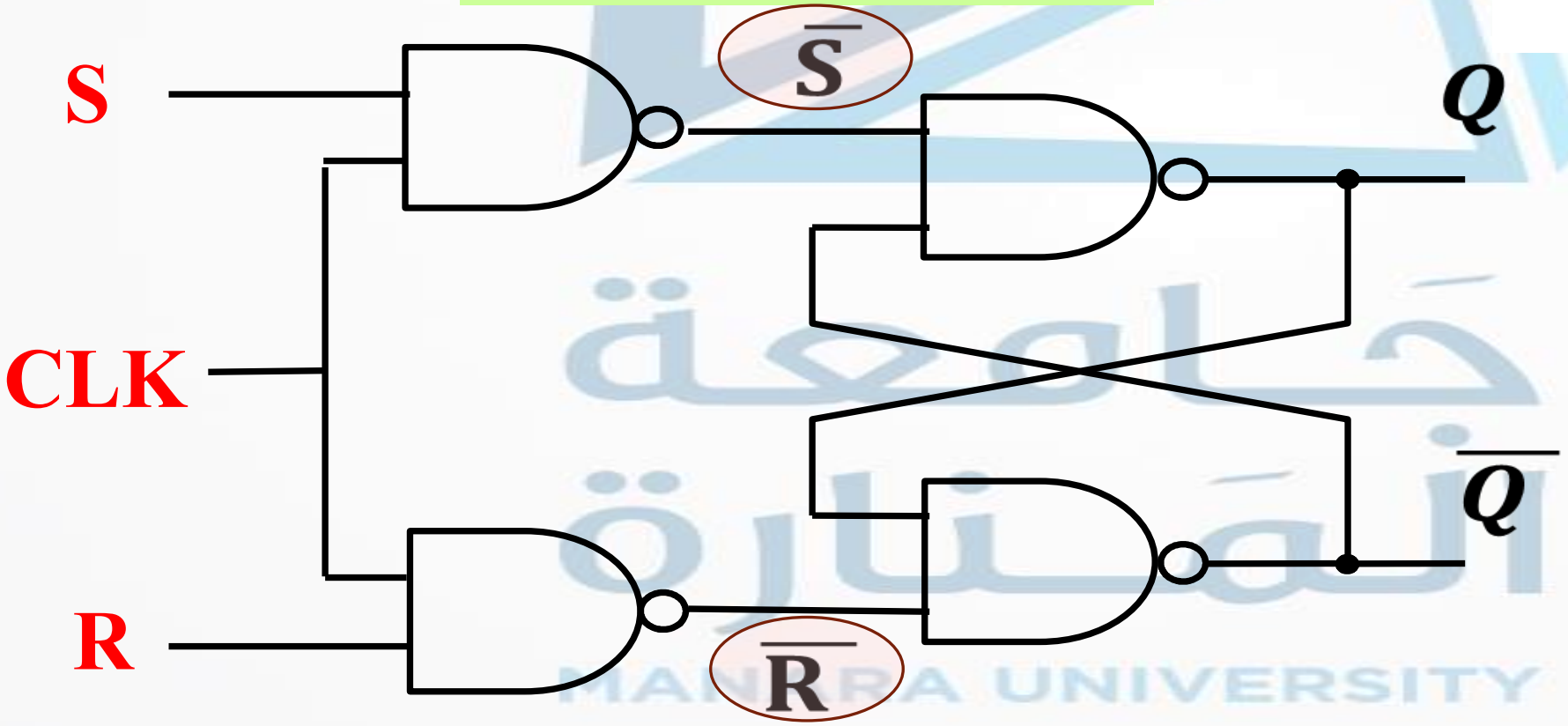
$$f = \frac{1.43}{(R_A + 2R_B)C}$$

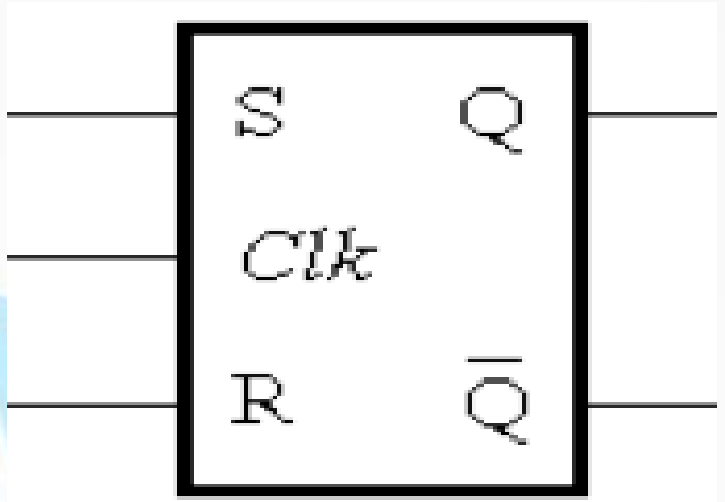
Gated SR latch with NAND gates



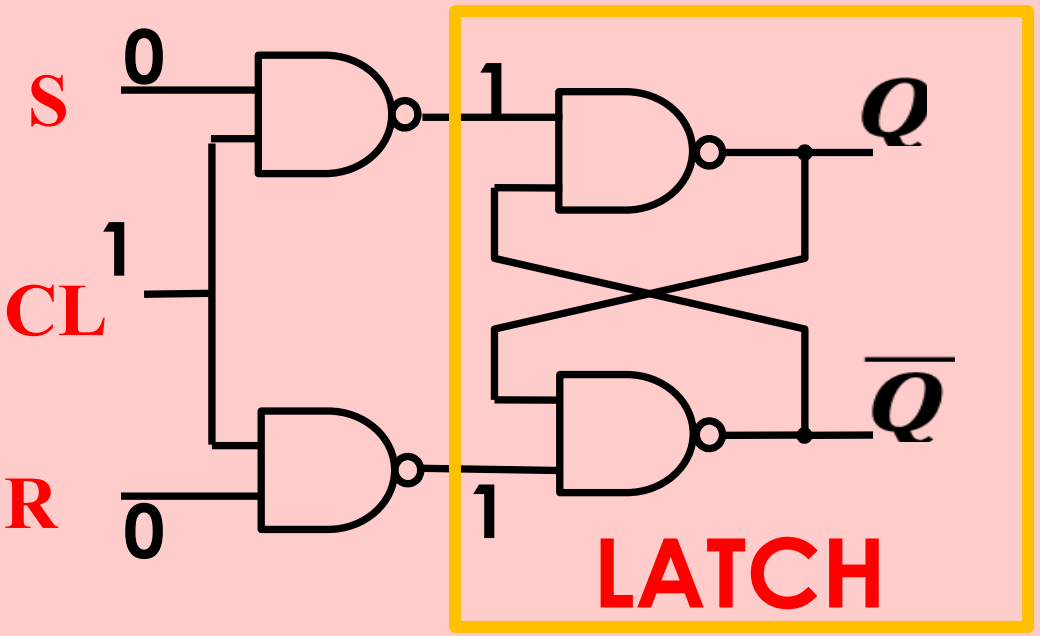
Circuit Diagram for the Gated SR Latch with NAND gates

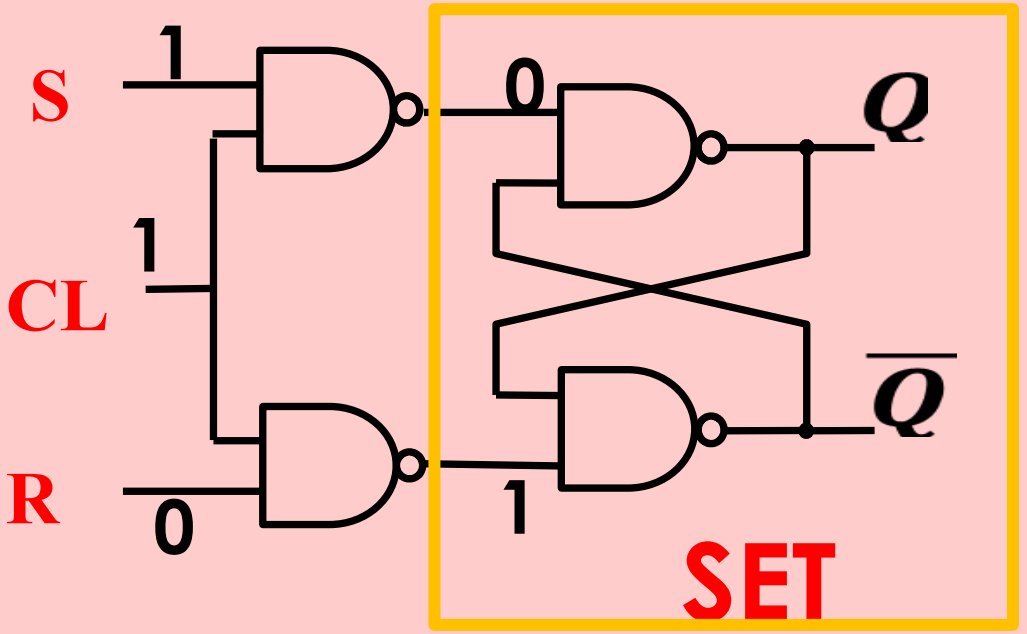
Circuit Diagram

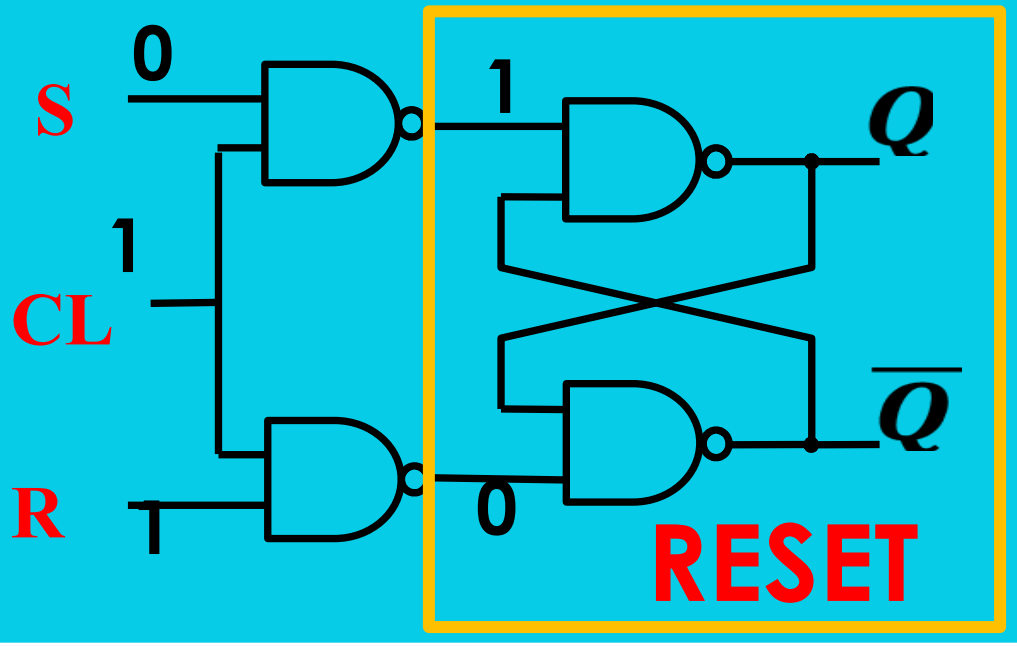


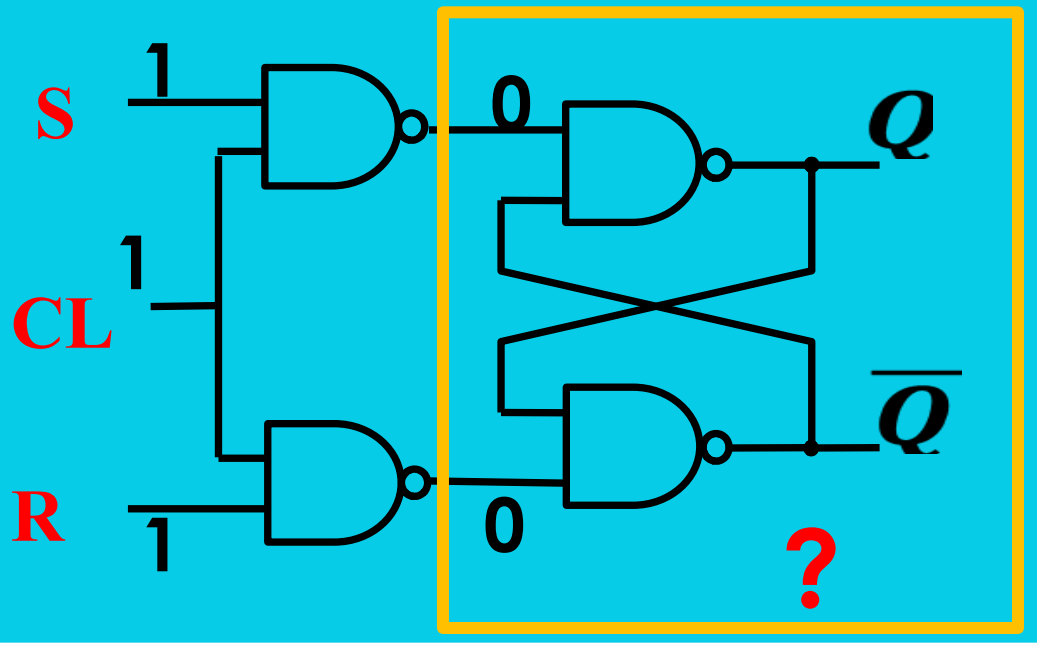


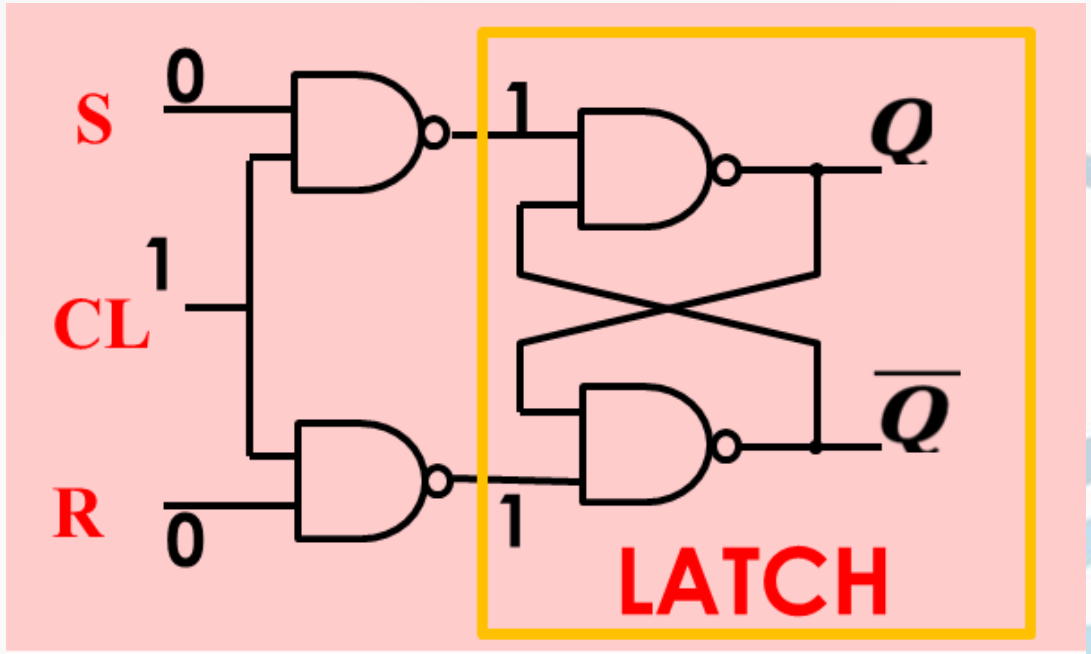
Graphical Symbol

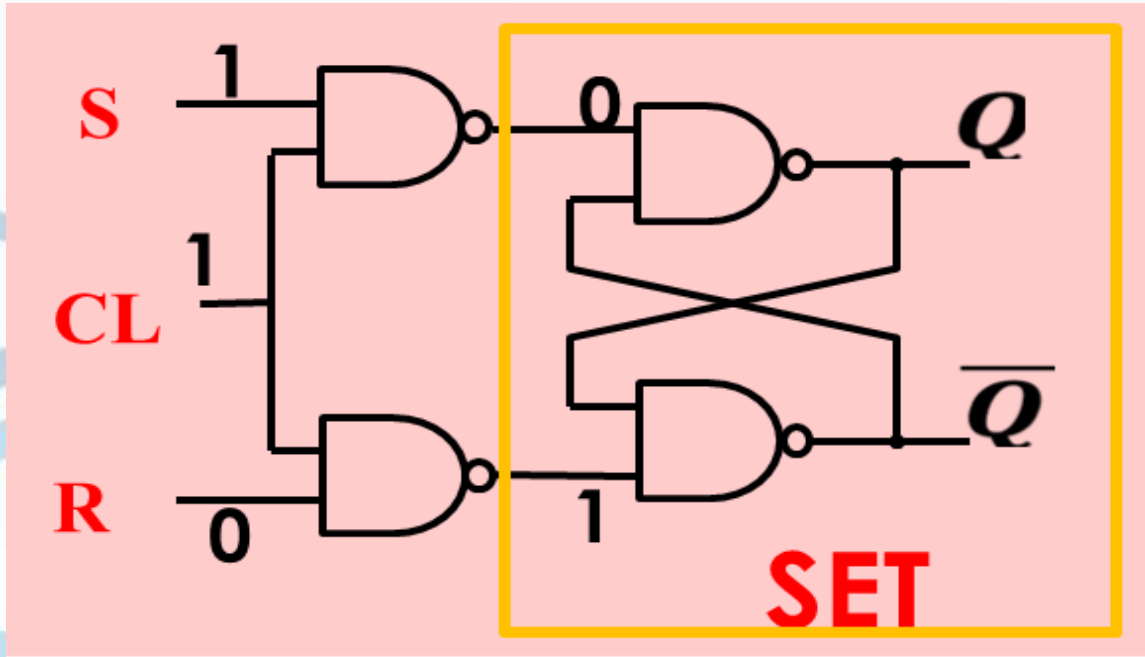

S
0
CL
1
R
0
1
1
Q
Q
LATCH

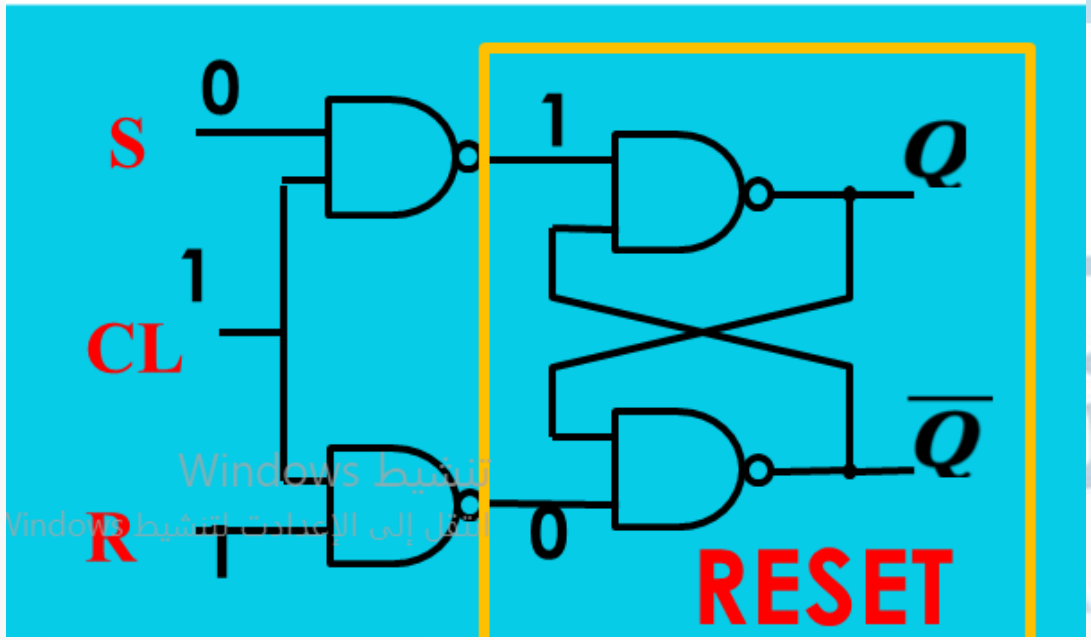

S
1
CL
1
R
0
0
Q
Q
1
SET

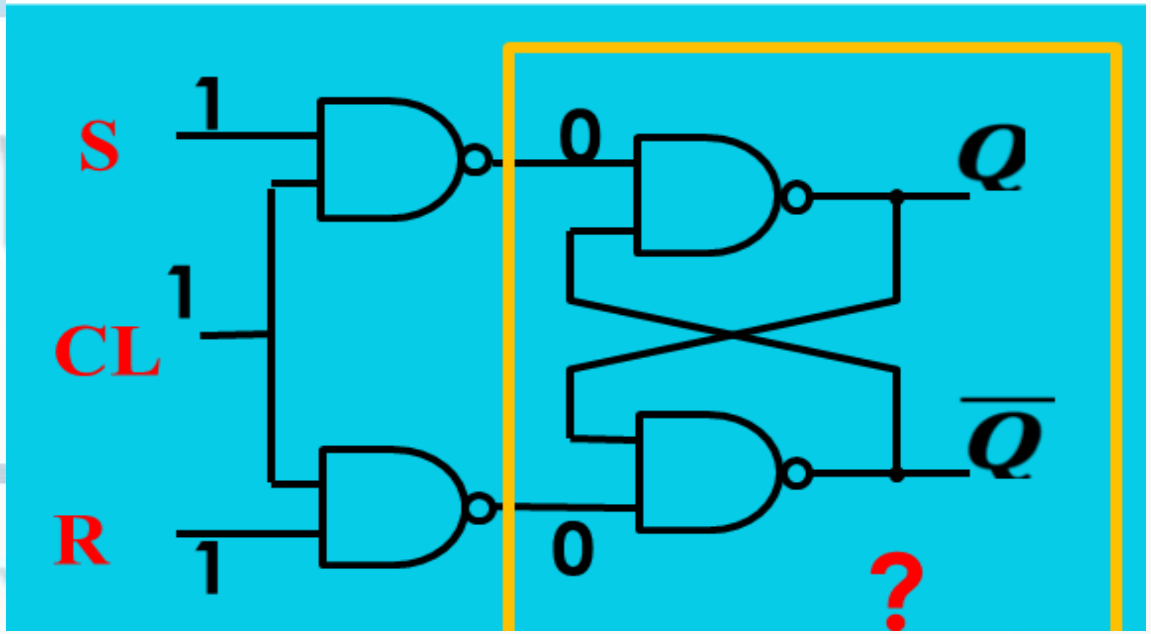

S
0
CL
1
R
1
1
Q
Q
0
RESET


S
1
CL
1
R
1
0
Q
Q
0
?





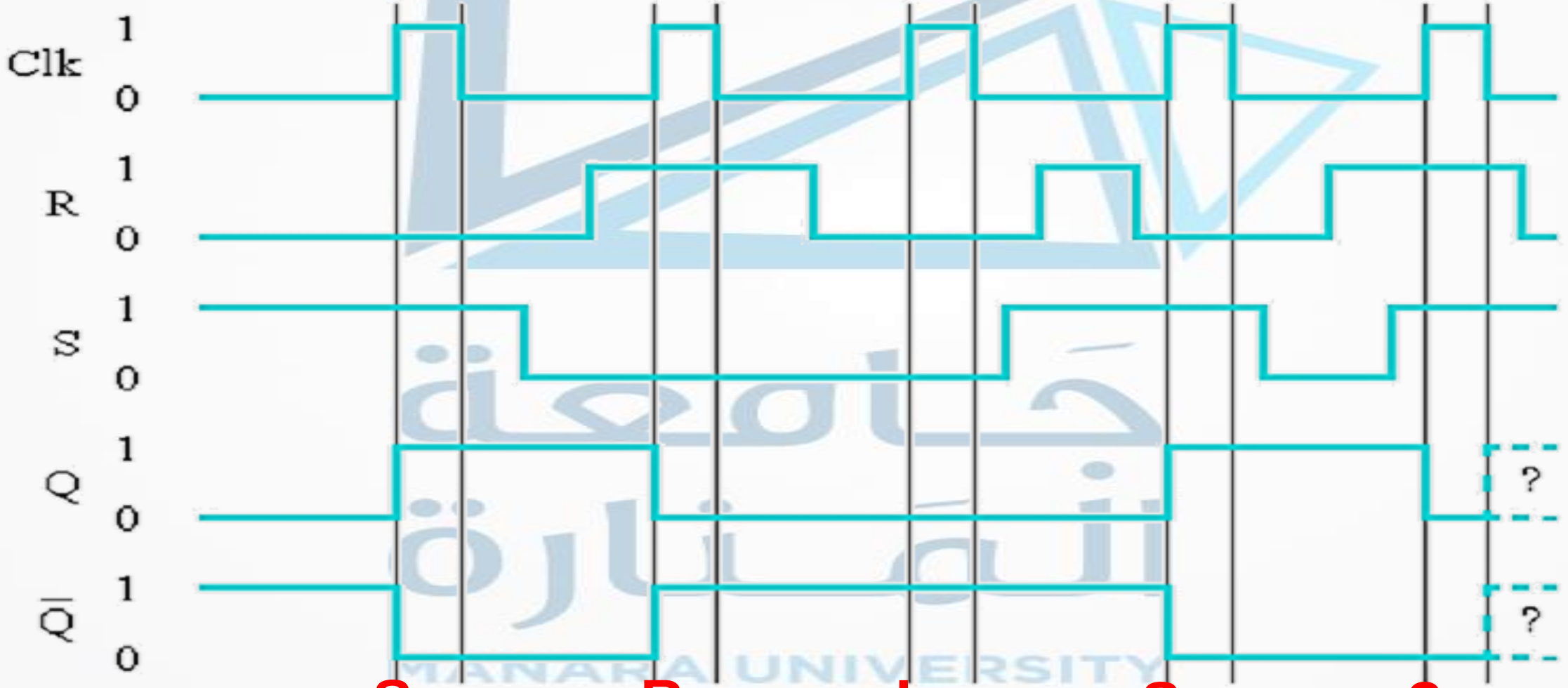




Characteristic Table
Gated SR Latch with NAND gates

CLK	S	R	Qa-	Qa+	Qb+	state
0	X	X	X	X	X	X
1	0	0	0	0	1	R=0 S=0 LAT
1	0	0	1	1	0	
1	0	1	0	0	1	R=1 S=0 RESET
1	0	1	1	0	1	
1	1	0	0	1	0	R=0 S=1 SET
1	1	0	1	1	0	
1	1	1	0	?	?	R=1 S=1 ?
1	1	1	1	?	?	

Timing Diagram for the Gated SR Latch



S R L S ?