Lecture 11

- Gated D Latch
- J-K FLIP FLOP
- T FLIP FLOP

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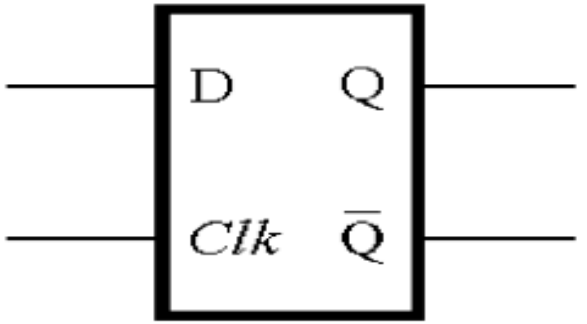
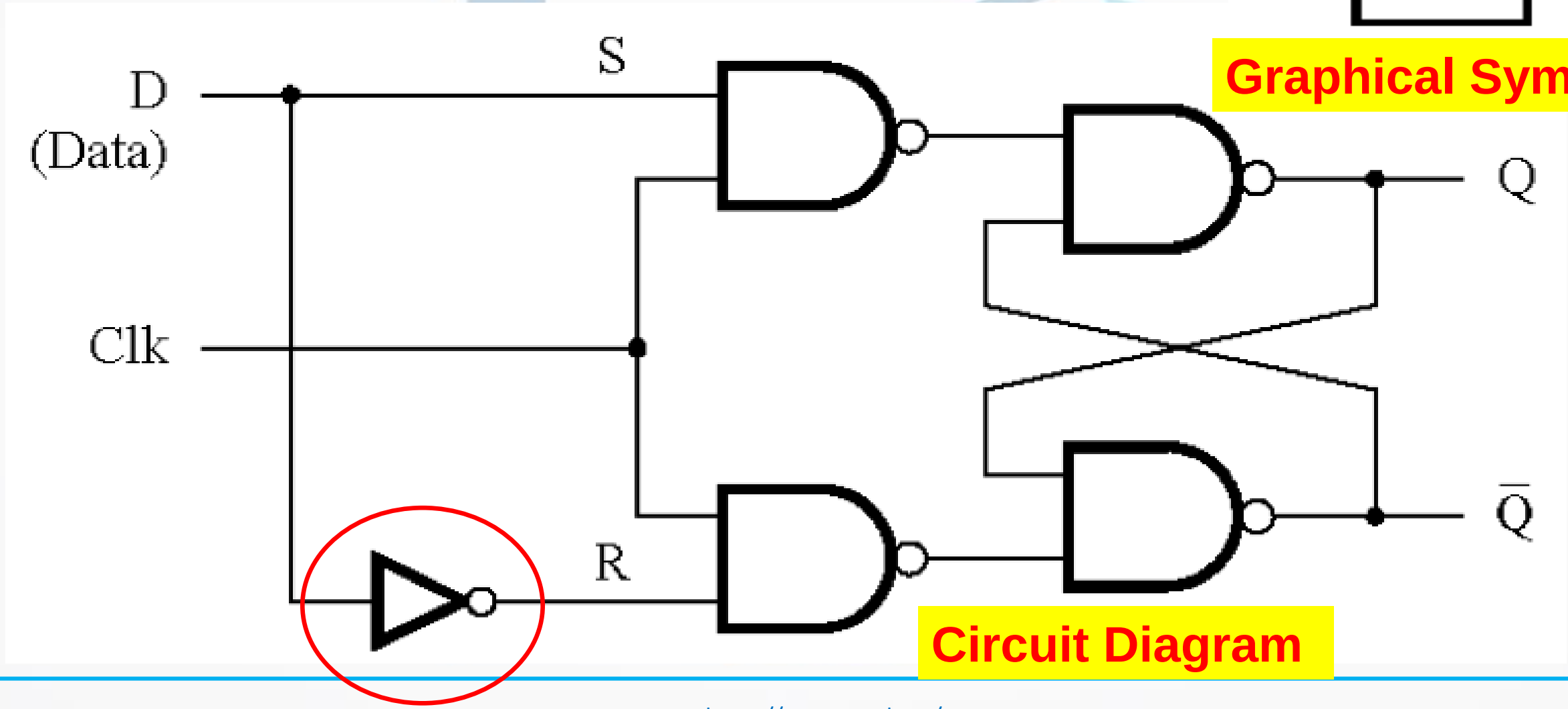
Motivation

- Dealing with two inputs (S and R) could be messy. For example, we may have to reset the latch before some operations in order to store a specific value but the reset may not be necessary depending on the current state of the latch.
- Why not just have one input and call it D.
- The D latch can be constructed using a simple modification of the SR latch.

Gated D Latch

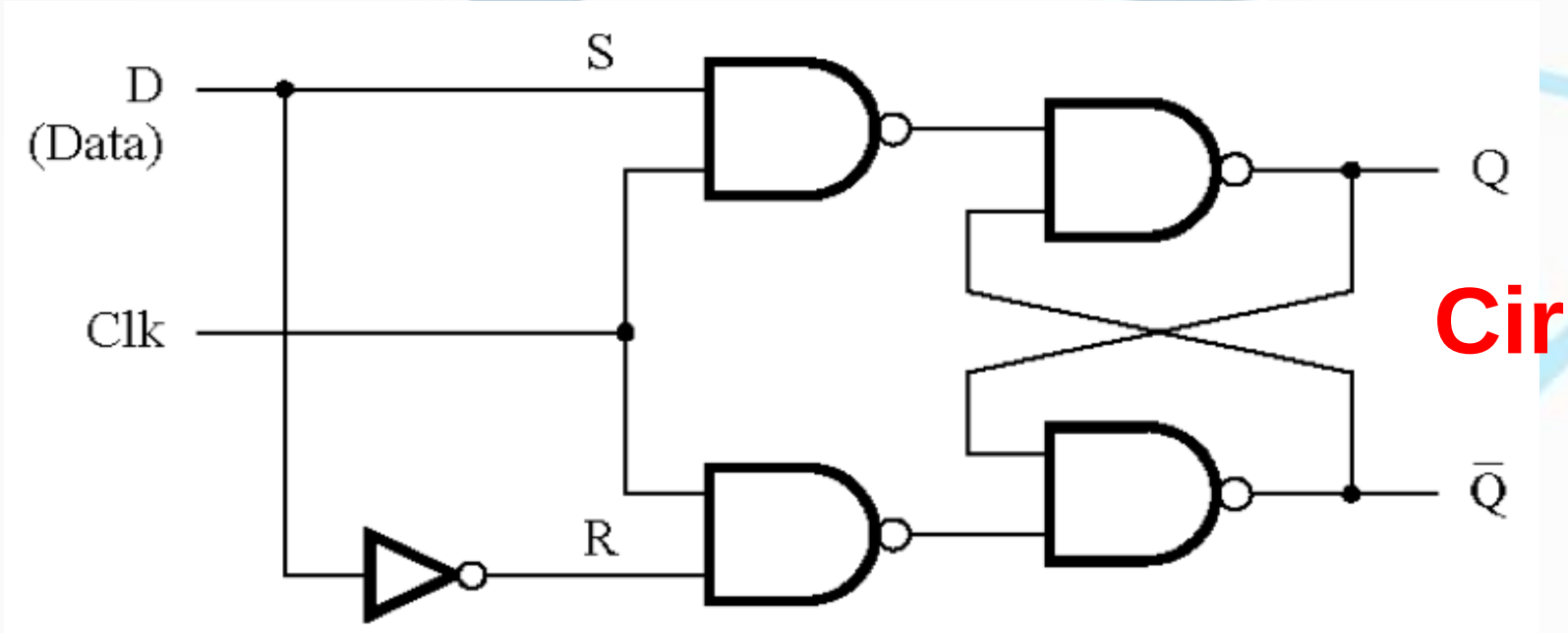


Graphical Symbol



Circuit Diagram

Circuit Diagram and Characteristic Table for the Gated D Latch



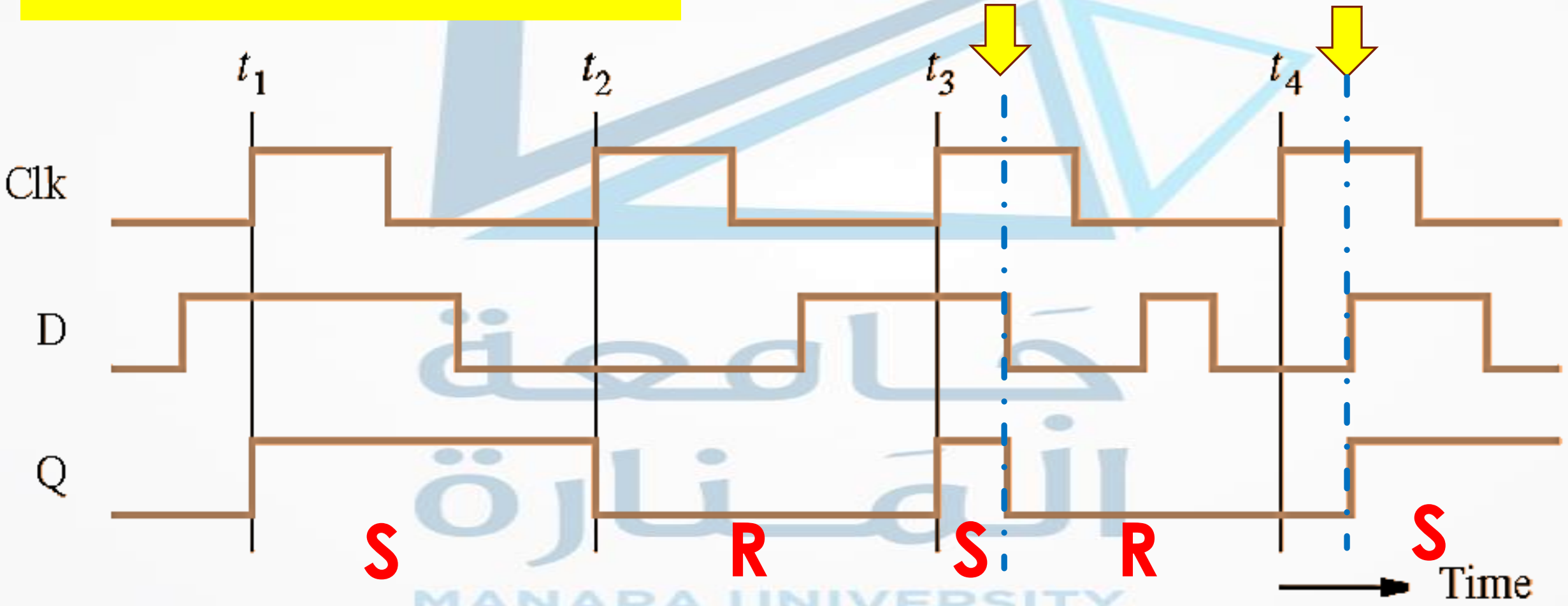
Circuit Diagram

Characteristic Table

Clk	D	$Q(t+1)$
0	x	$Q(t)$
1	0	0
1	1	1

Note that it is now impossible to have S=R=1.

Timing Diagram for the Gated D Latch

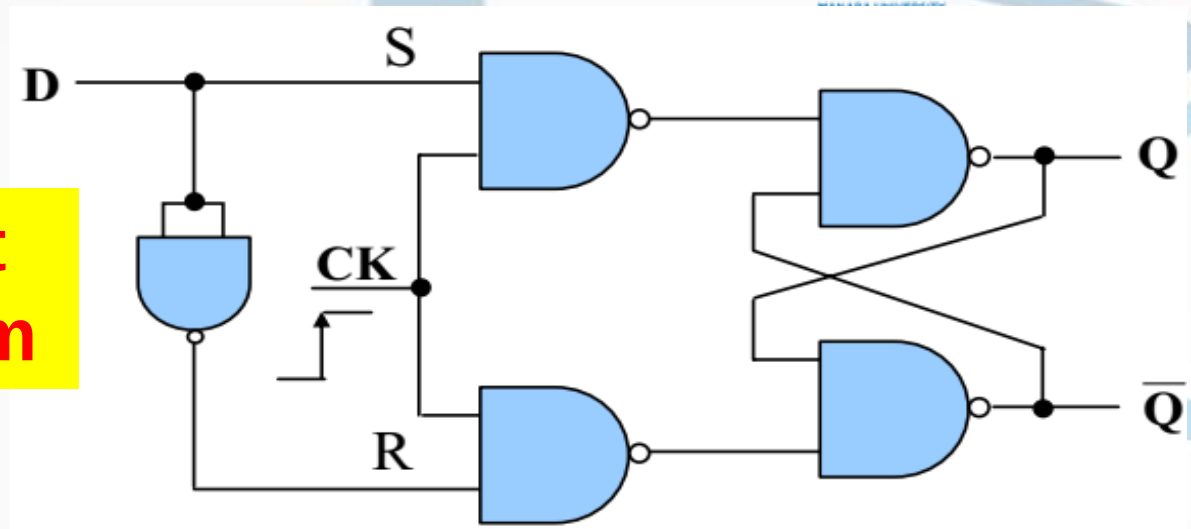


D-Type Flip-Flop

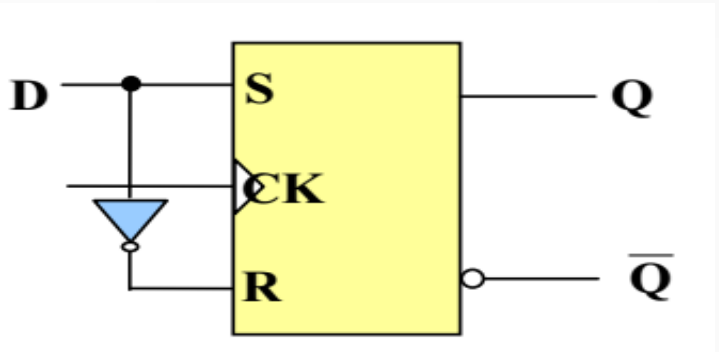
دائرة القلاب من النوع D

جَامعة المَنارة

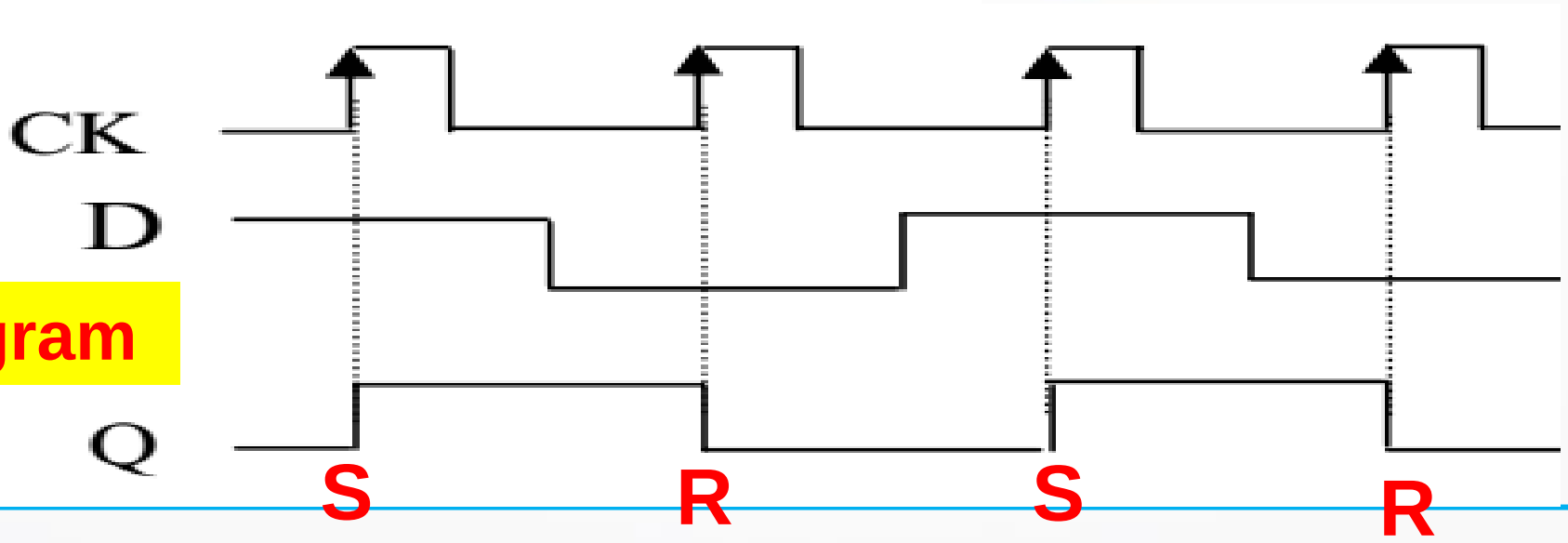
Circuit Diagram



Graphical Symbol



Timing Diagram

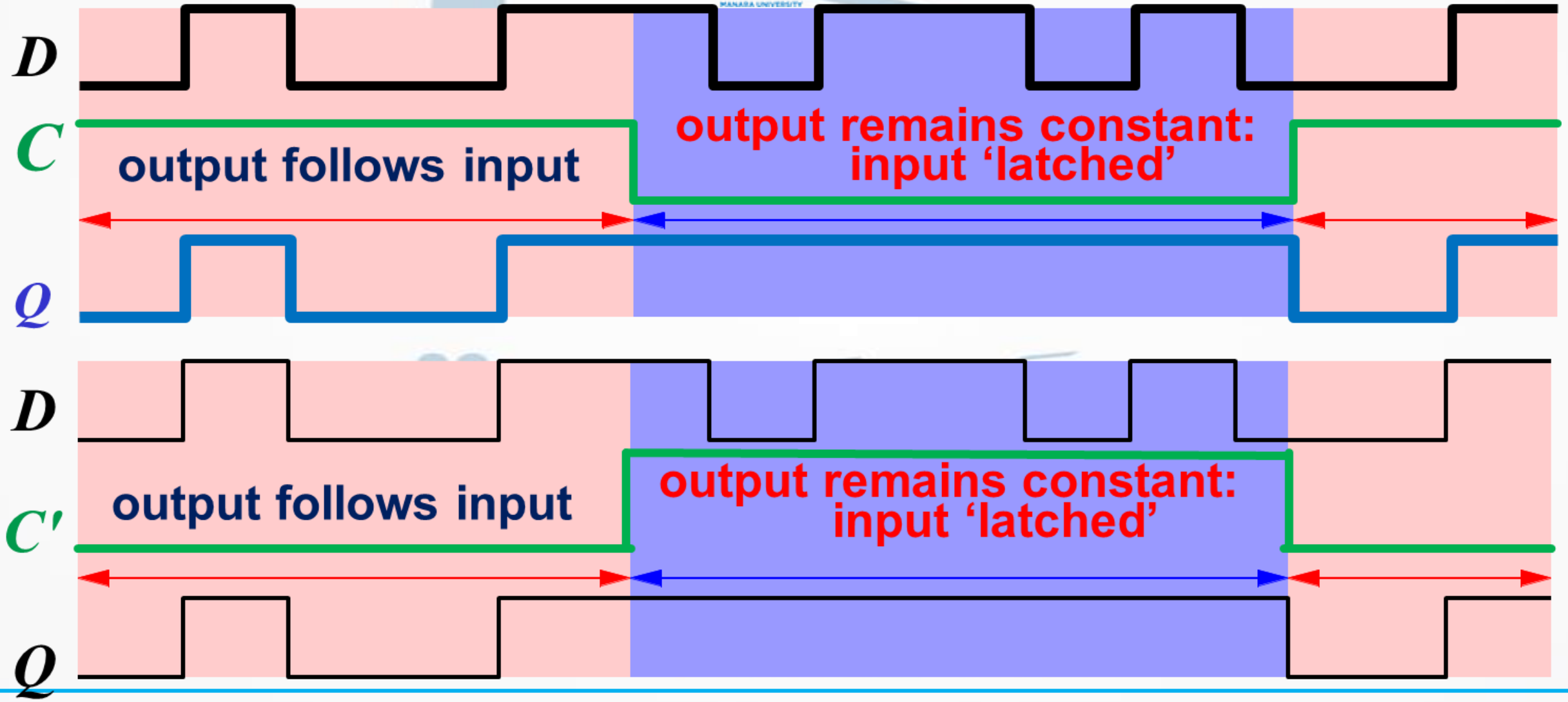


Characteristic Table
Gated D Latch

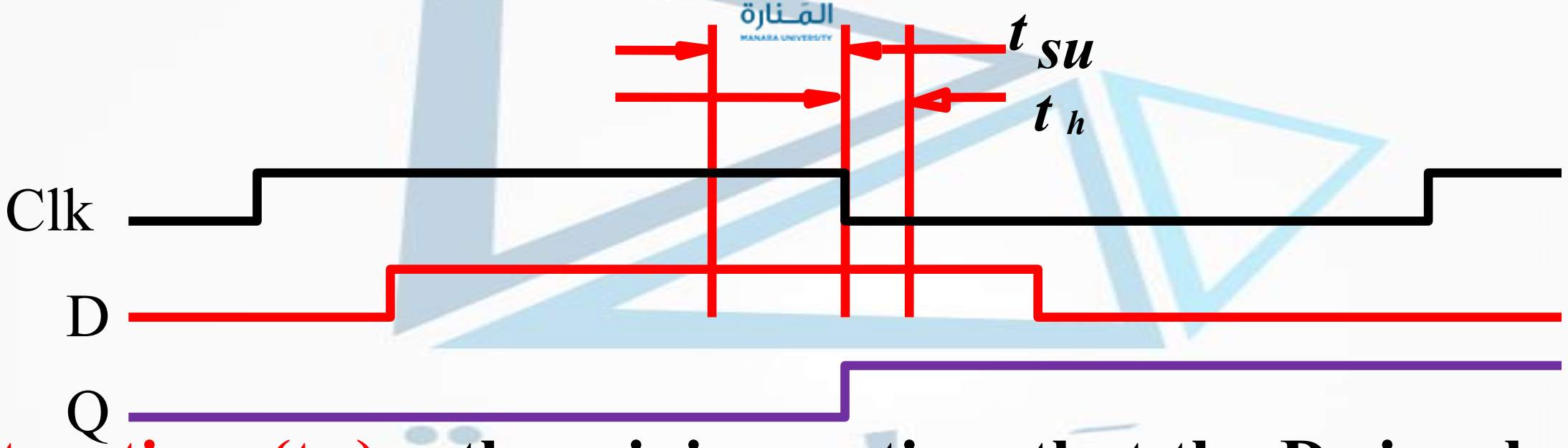
المدخلات		الخرج	وضع التشغيل
D	CK	Q	(Mode of Operation)
1	↑	1	الحالة الفعالة (SET) (stores a 1)
0	↑	0	الحالة الغير فعالة (RESET) (stores a 0)

↑ = نبضة الساعة تتغير من (0) الى (1)

Timing Diagram for the Gated D Latch



Setup and hold times



Setup time (t_{su}) – the minimum time that the D signal must be stable prior to the negative edge of the Clock signal.

Hold time (t_h) – the minimum time that the D signal must remain stable after the negative edge of the Clock signal.

J-K FLIP FLOP

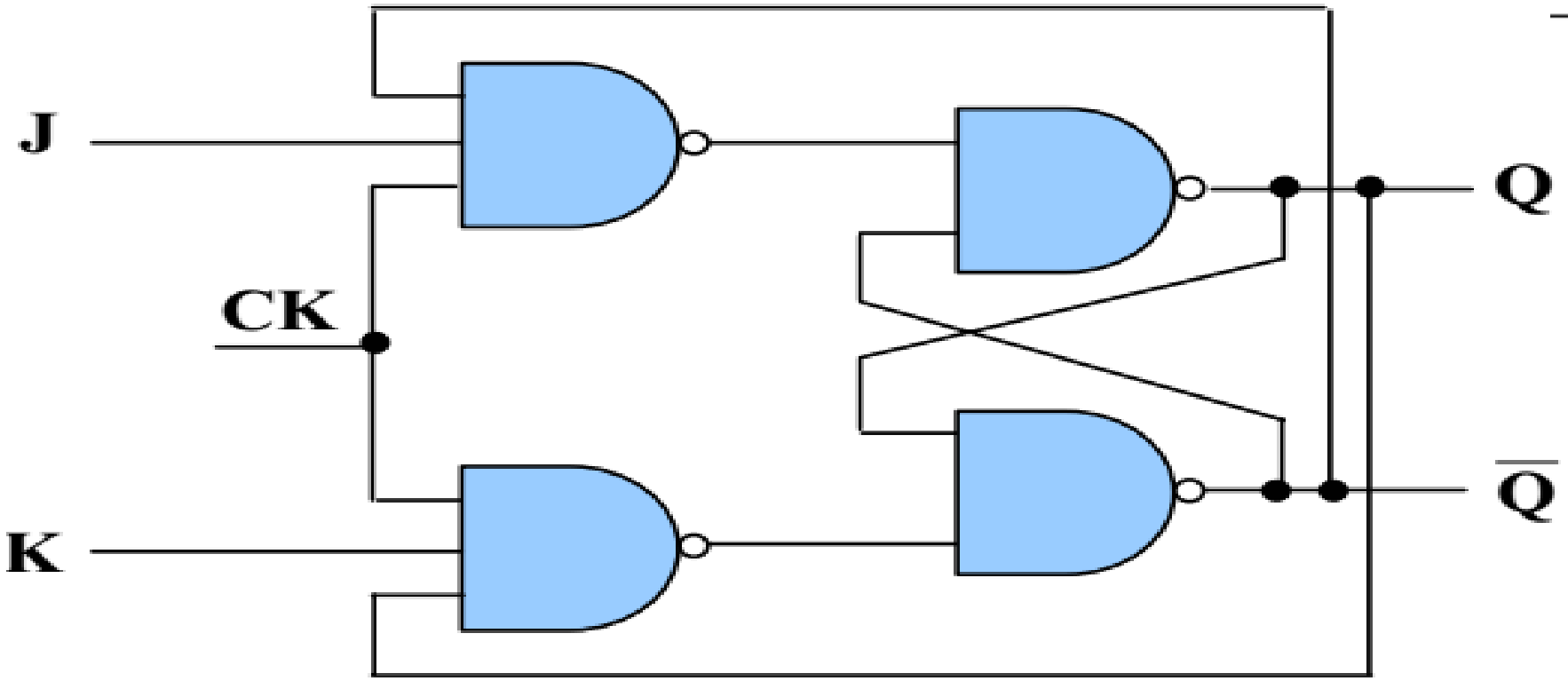
- The ***JK flip-flop*** can also be derived from the basic D flip-flop such that

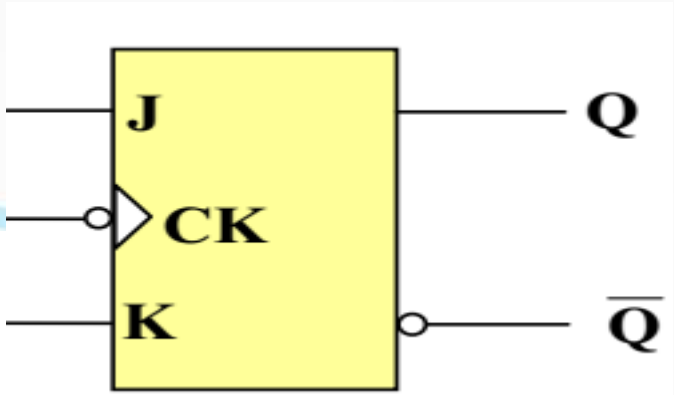
  $D=JQ'+K'Q$

- The JK flip-flop combines aspects of the SR and the T flip-flop
  - It behaves as the SR flip-flop (where J=S and K=R) for all values except J=K=1
  - For J=K=1, it toggles like the T flip-flop

J-K FLIP FLOP

Circuit Diagram





Graphical Symbol

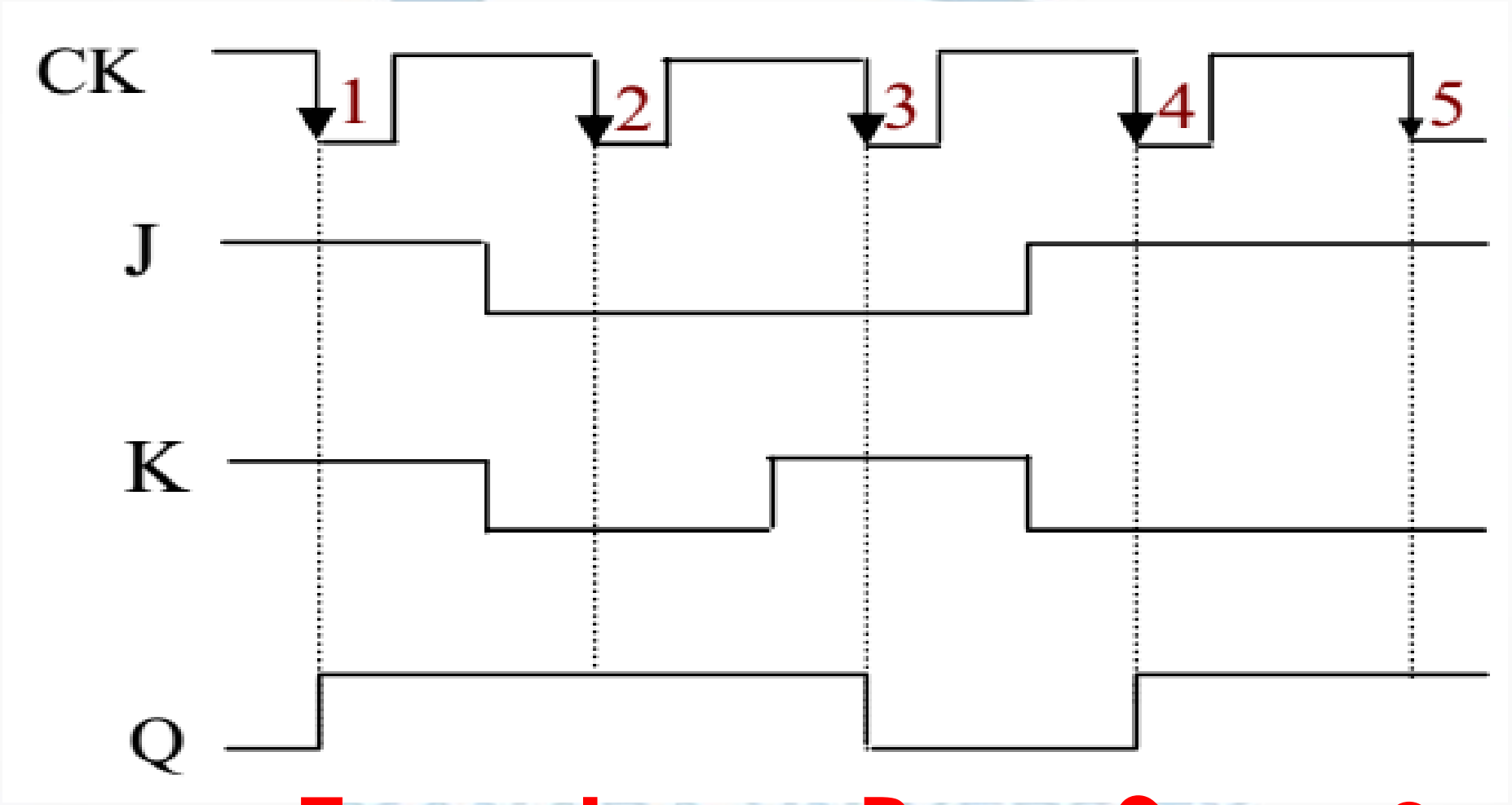
Characteristic Table
J-K FLIP FLOP

المدخلات			الخرج	وضع التشغيل (Mode of Operation)
J	K	CK	Q	
0	0	↓	Q_0	وضع الإمساك (عدم التغير) No Change
0	1	↓	0	الوضع غير الفعال (RESET)
1	0	↓	1	الوضع الفعال (SET)
1	1	↓	$\overline{Q}_0$	وضع التبديل Toggle

↓ = نبضة الساعة تتغير من (1) الى (0)

Q_0 = الخرج الموجود قبل وصول أول نبضة تزامن

Timing Diagram for J-K FLIP FLOP

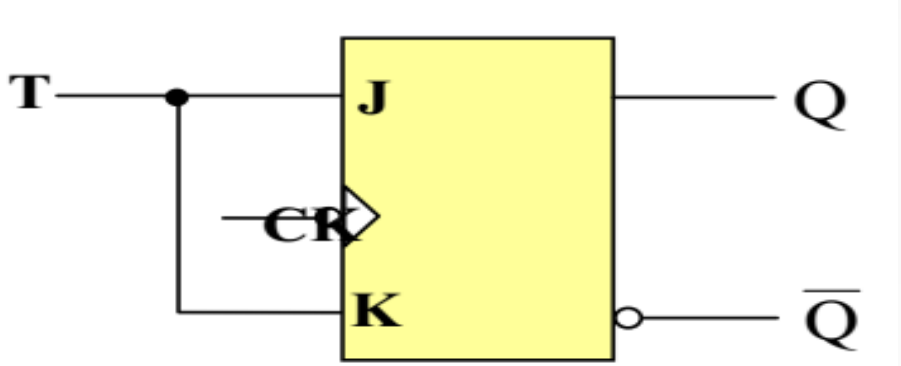


T L R S S

T FLIP FLOP

T FLIP FLOP

Characteristic Table
T FLIP FLOP



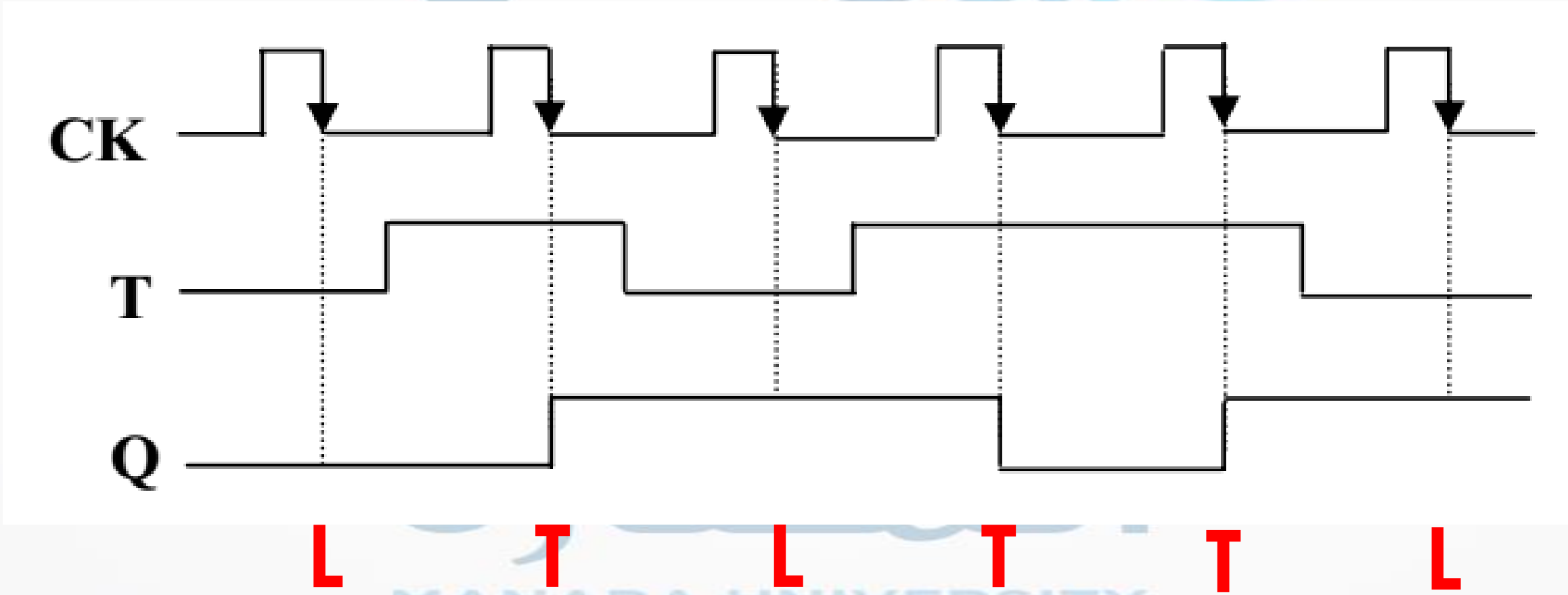
Graphical Symbol

المدخلات		الخرج	وضع التشغيل (Mode of Operation)
T	CK	Q	
0	↓	Q_0	وضع الإمساك (عدم التغير) No Change
1	↓	$\overline{Q}_0$	وضع التبديل Toggle

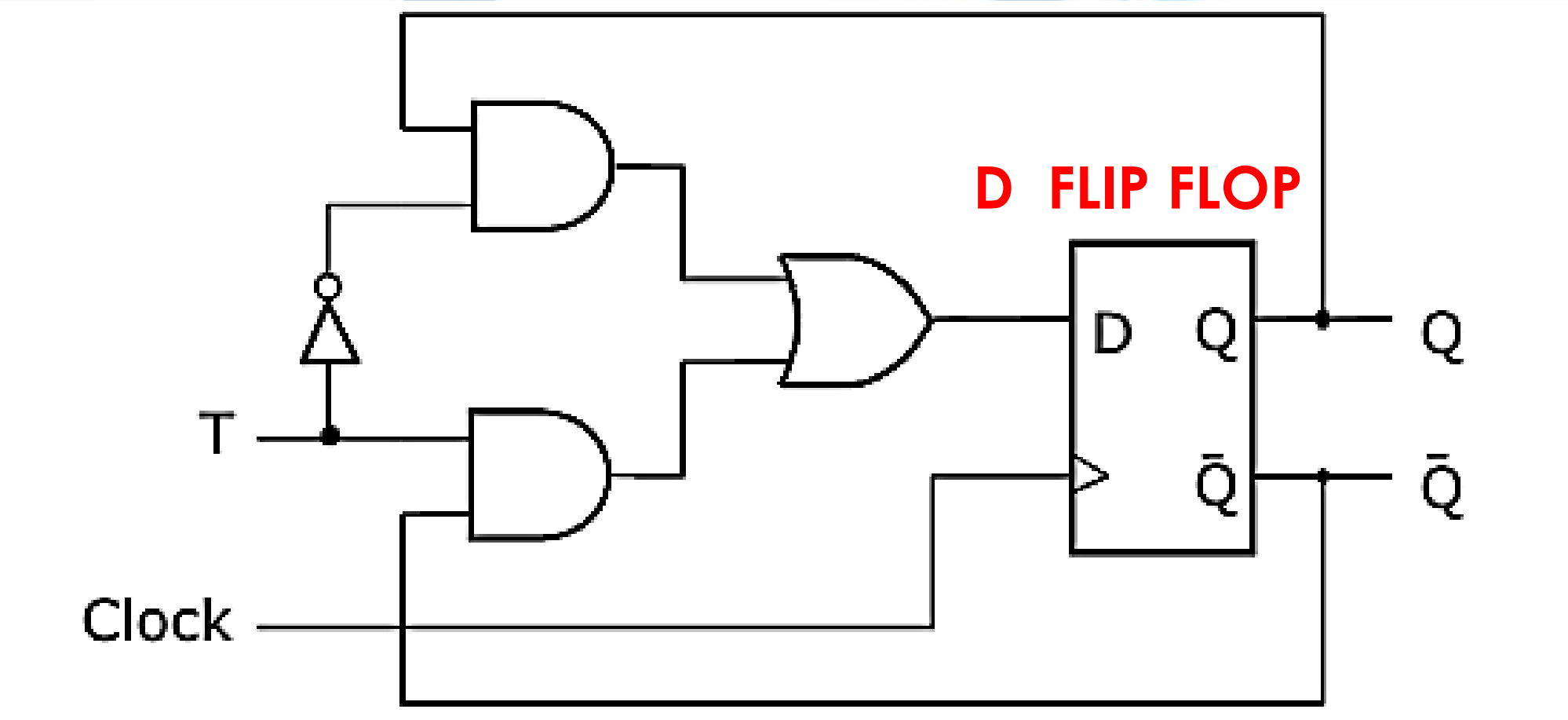
↓ = نبضة الساعة تتغير من (1) الى (0)

Q_0 = الخرج الموجود قبل وصول أول نبضة تزامن

Timing Diagram
T FLIP FLOP

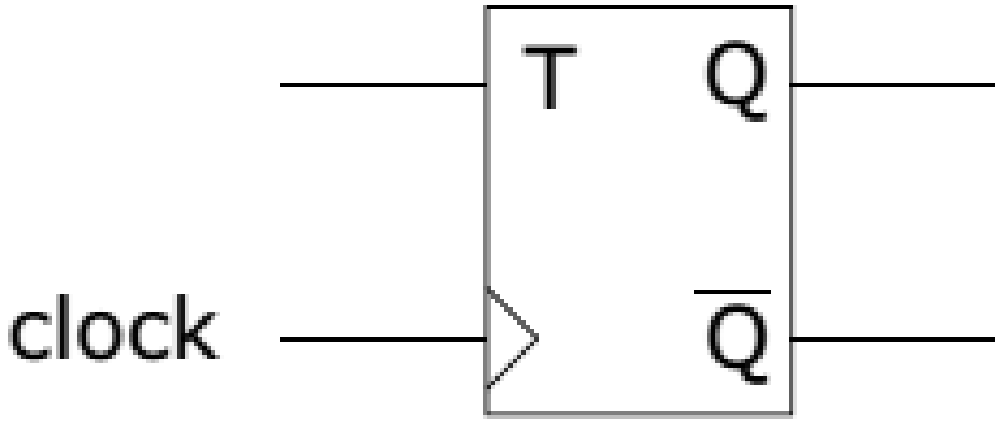


T FLIP FLOP
Using D FLIP FLOP



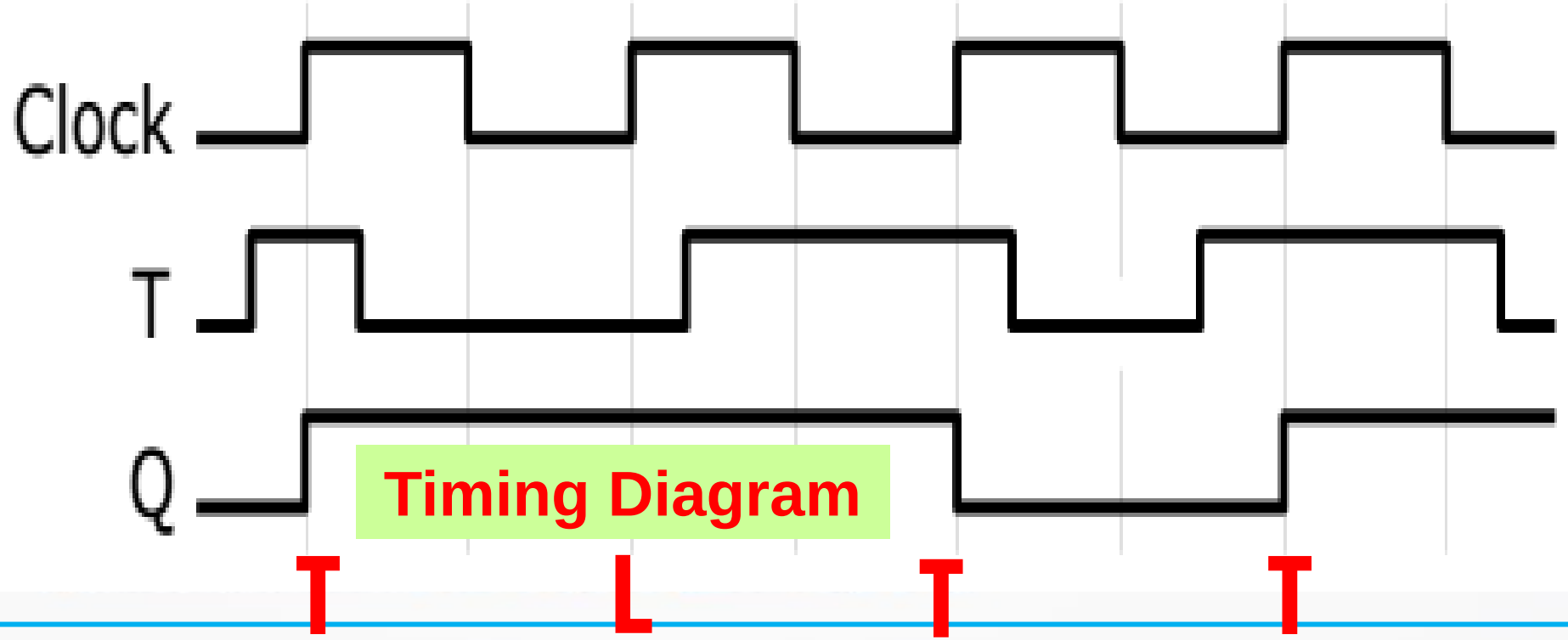
Timing Diagram
T FLIP FLOP

Positive edge triggered



Graphical Symbol

T	Q(t+1)
0	Q(t)
1	Q′(t)

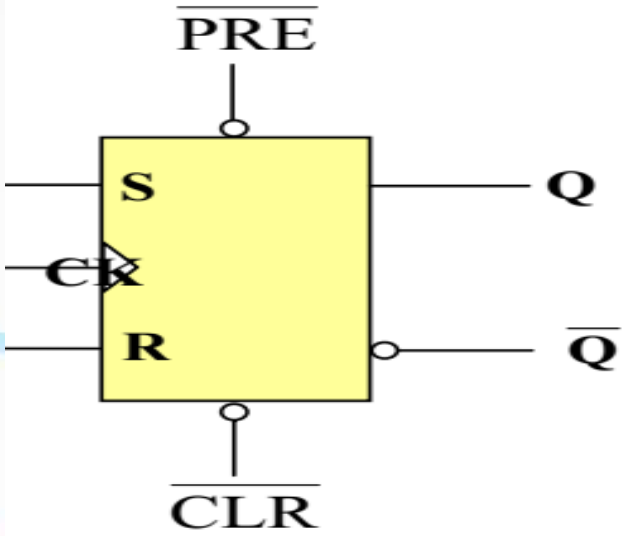


Timing Diagram

- The name T derives from the behavior of the circuit, which 'toggles' its state when T=1
  - This feature makes the T flip-flop a useful element when constructing counter circuits

CLEAR AND PRESET INPUTS

Graphical Symbol



Characteristic Table
Gated SR Latch

المدخلات					الخرج	وضع التشغيل
$\overline{PRE}$	$\overline{CLR}$	CK	S	R	Q	(Mode of Operation)
0	1	X	X	X	1	(SET) الوضع الفعال
1	0	X	X	X	0	(RESET) الوضع غير الفعال
0	0	X	X	X	?	حالة الحظر

state diagram of flip flop