

Lecture 16

Shift Registers
مسجلات الازاحة

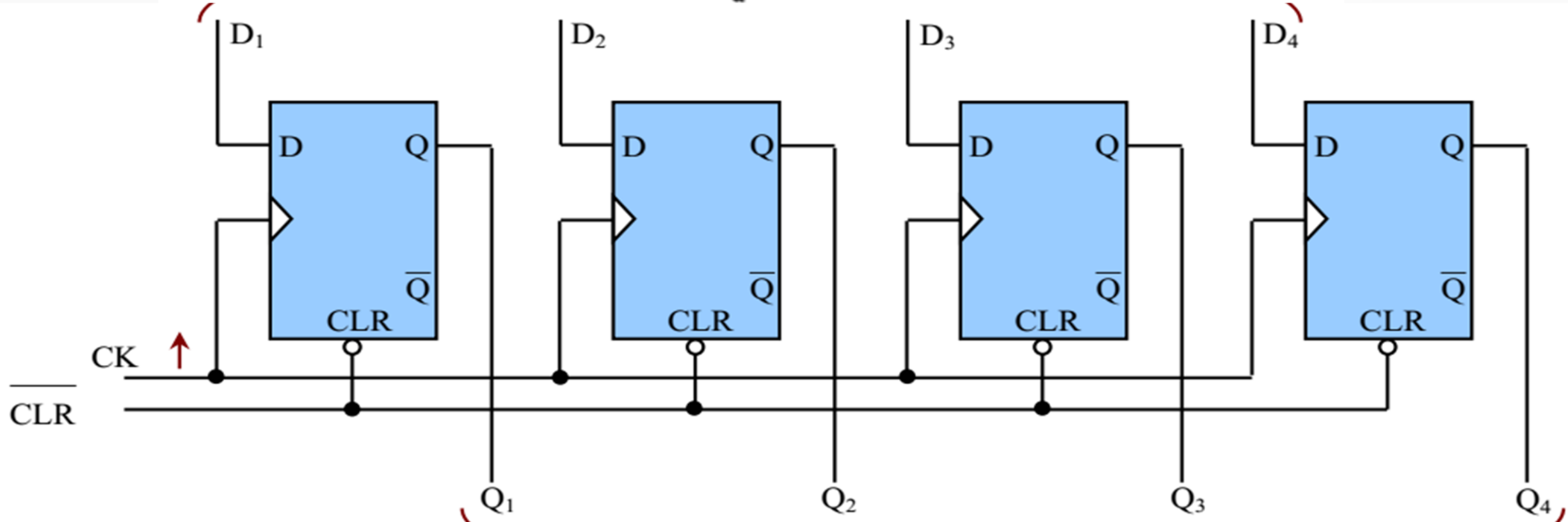
Dr. Bassam Atieh

MANARA UNIVERSITY

BUFFER Registers

مسجلات العزل

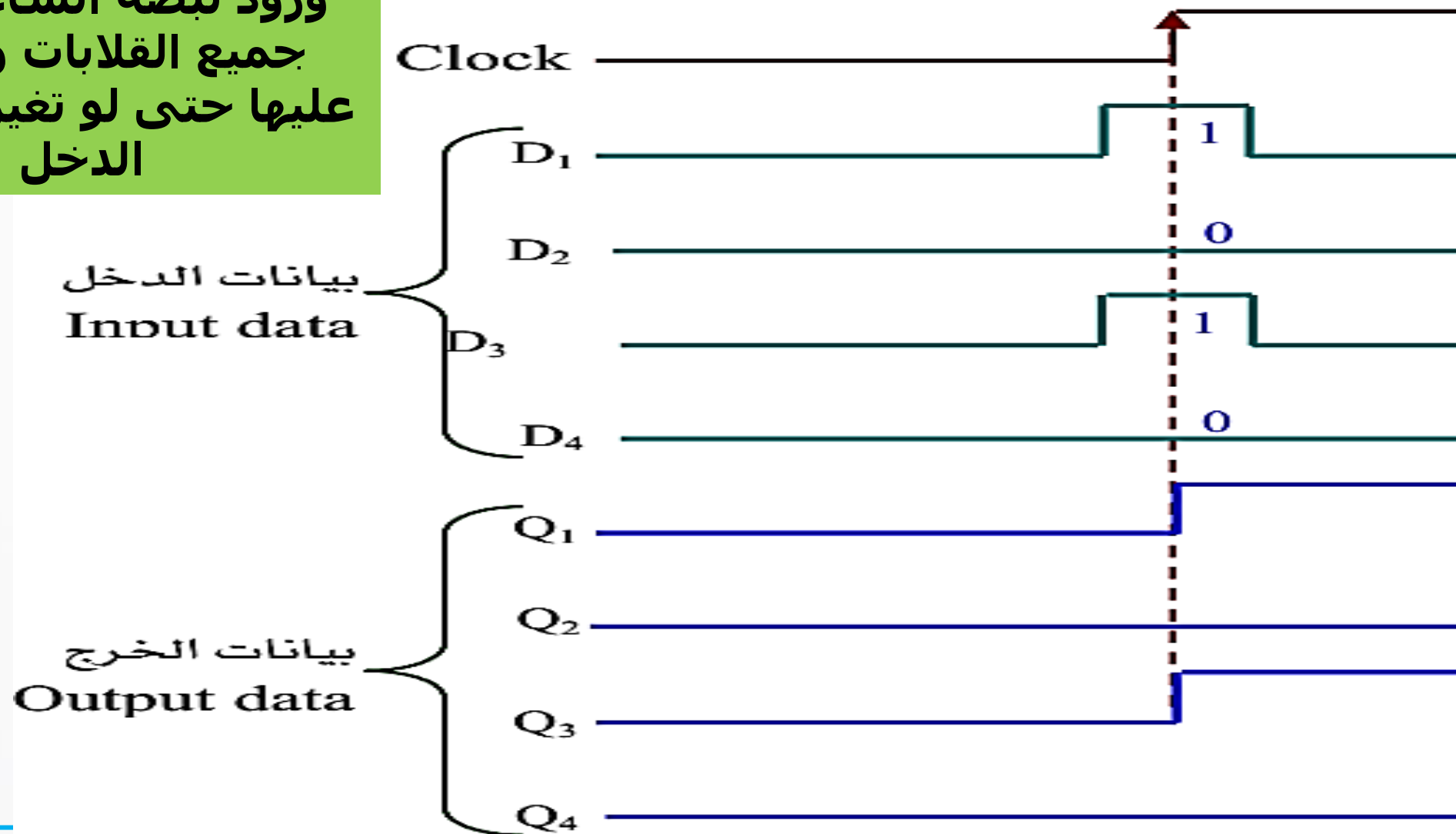
البيانات المطلوب تخزينها على التوازي (4-bit word to be stored)



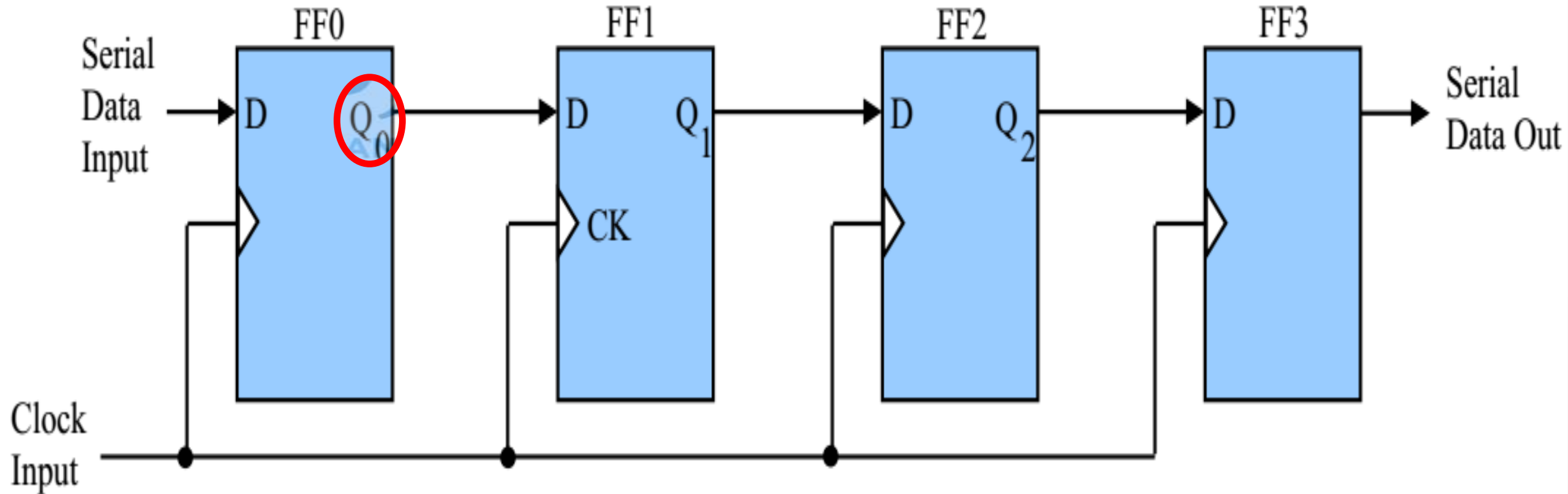
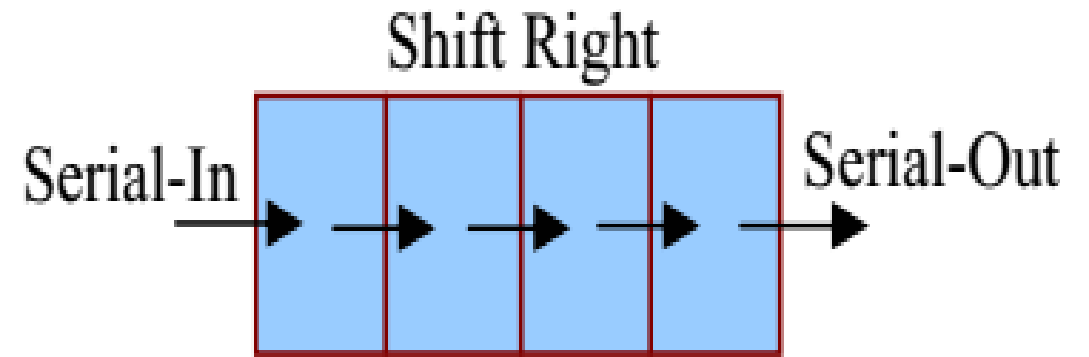
خرج البيانات على التوازي (parallel data outputs)

Timing Diagram

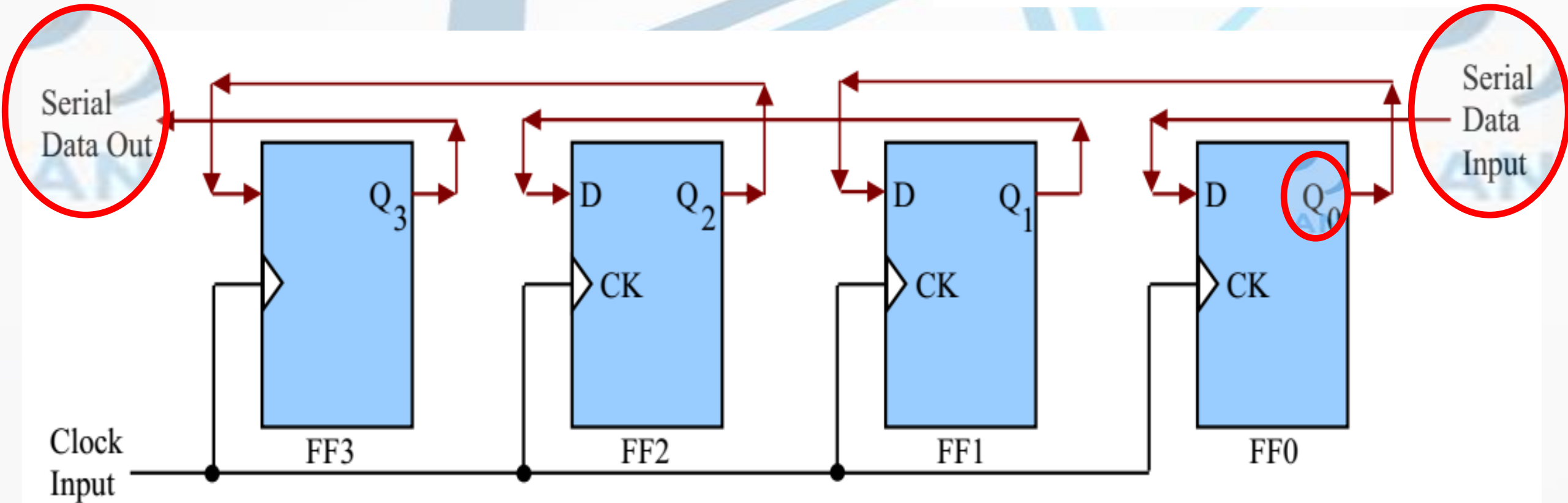
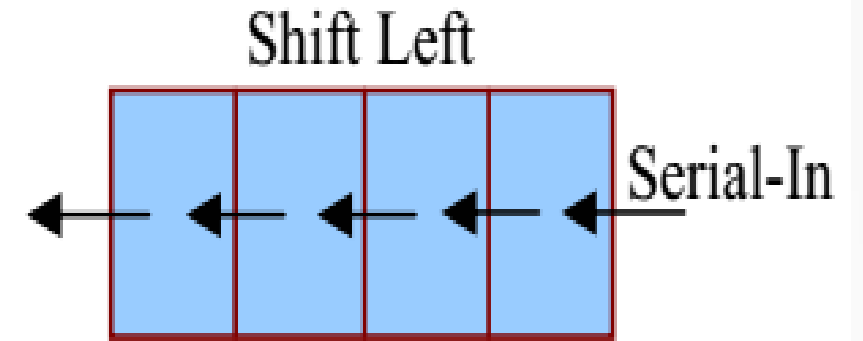
لاحظ ان بيانات الخرج سوف
تطابق بيانات الدخل عن
ورود نبضة الساعة على
جميع القلابات وتحافظ
عليها حتى لو تغيرت بيانات
الدخل



Serial-in, Serial-out (SISO) Shift Right Registers



Serial-in, Serial-out (SISO) Shift Left Registers



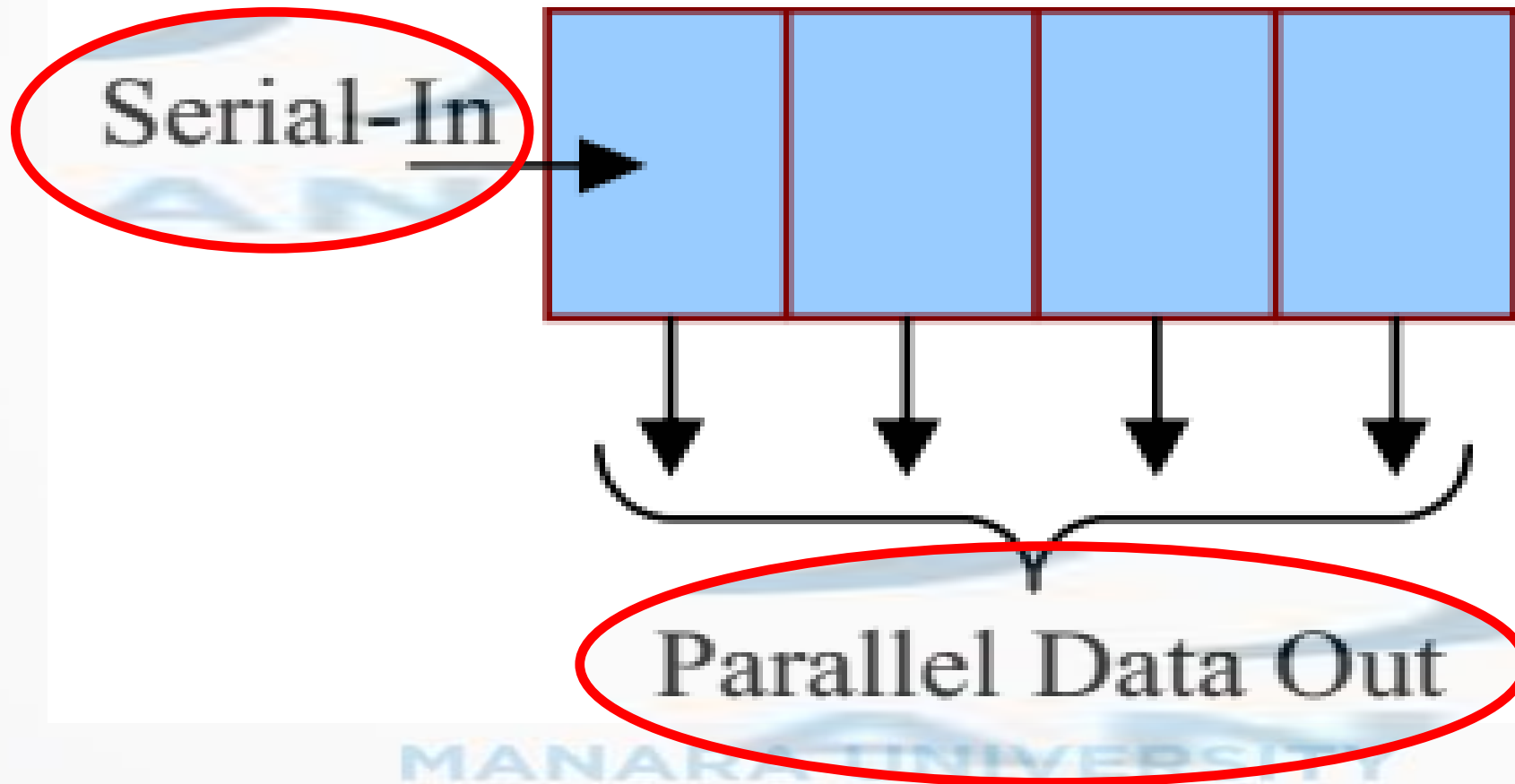
Serial-in, Serial-out (SISO) Shift Registers

نبضات التزامن	البيانات المراد تخزينها	خرج المسجل			
Clock	Input	Q ₀	Q ₁	Q ₂	Q ₃
—	—	0	1	1	0
1 st	1	1	0	1	1
2 nd	0	0	1	0	1
3 rd	0	0	0	1	0
4 th	1	1	0	0	1

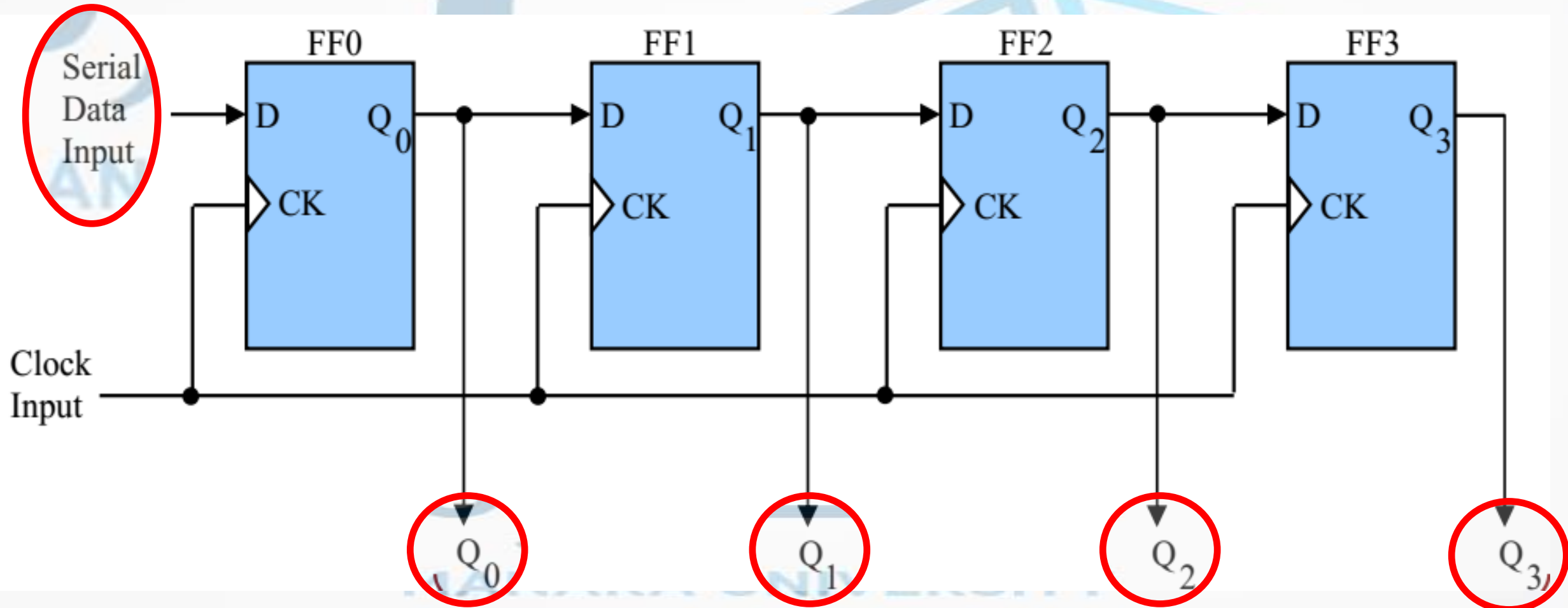
بيانات الداخل

بيانات الخرج بعد 4 نبضات

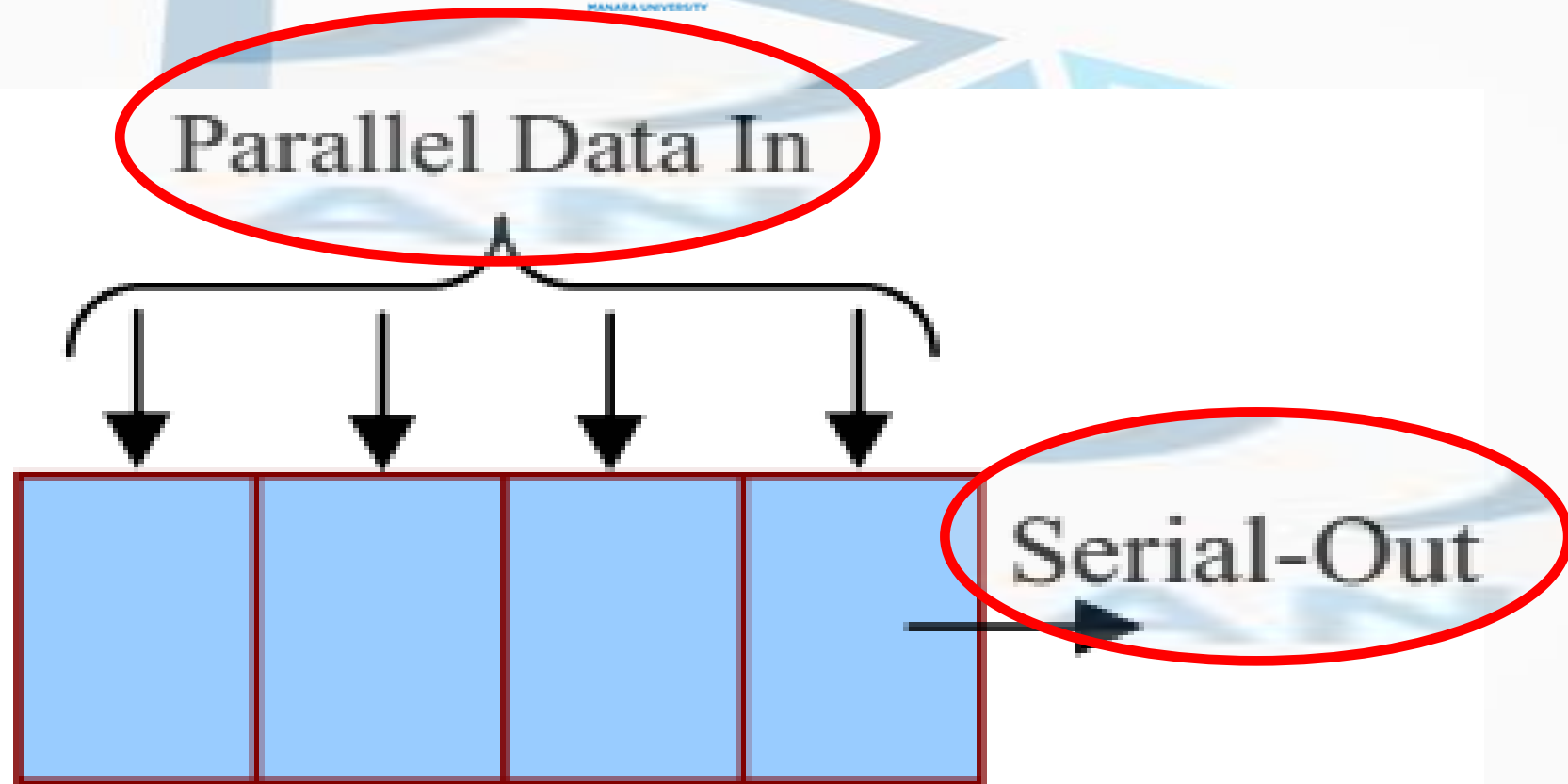
Serial-in, Parallel-out (SIPO) Shift Registers



Serial-in, Parallel-out (SIPO) Shift Registers

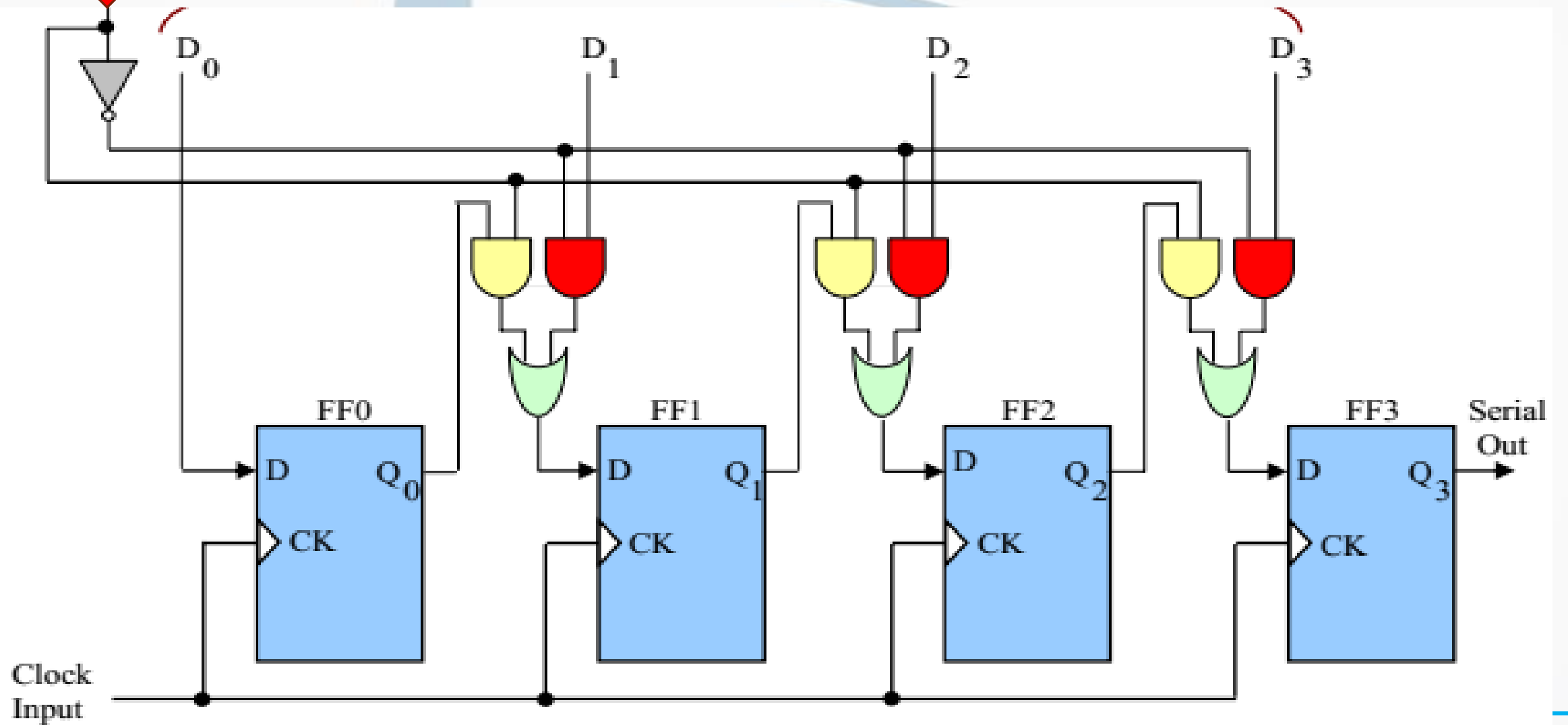


Parallel-in, Serial-out (PISO) Shift Registers

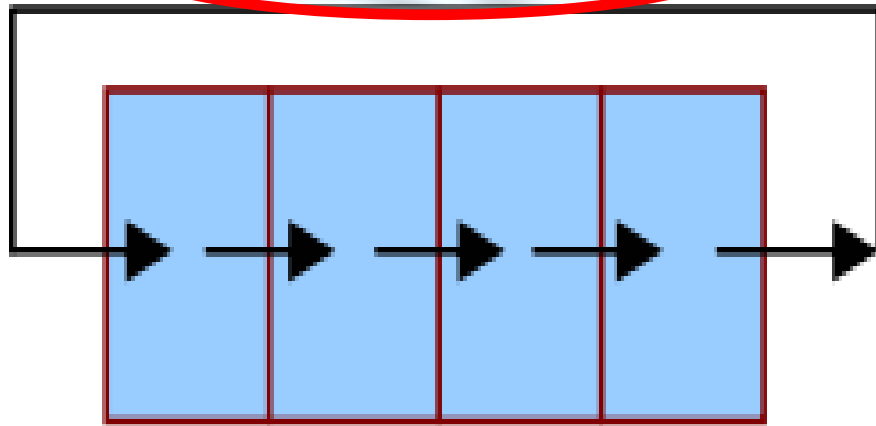


1 for Shift , 0 for load

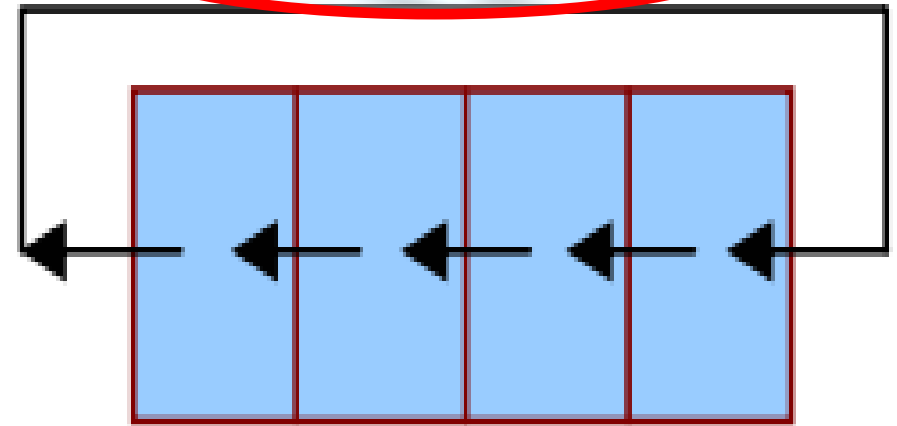
Parallel-in, Serial-out (PISO) Shift Registers

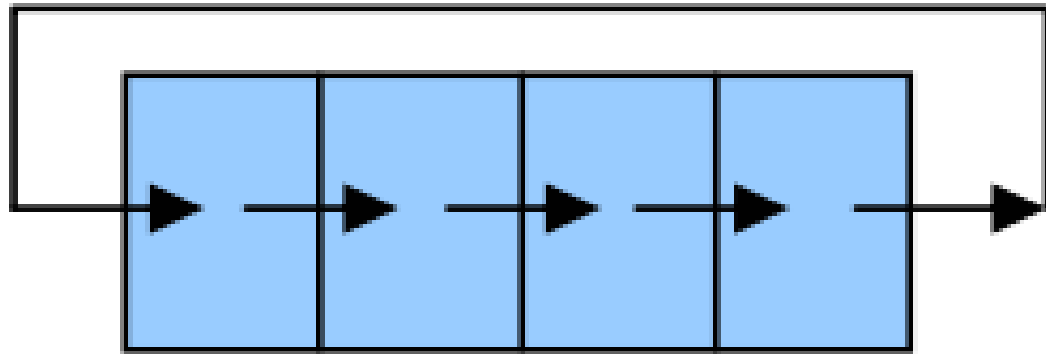


Rotate Right

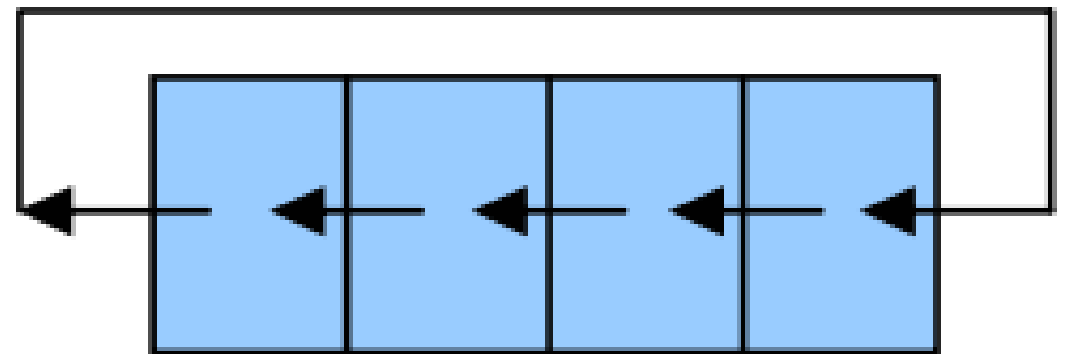


Rotate Left





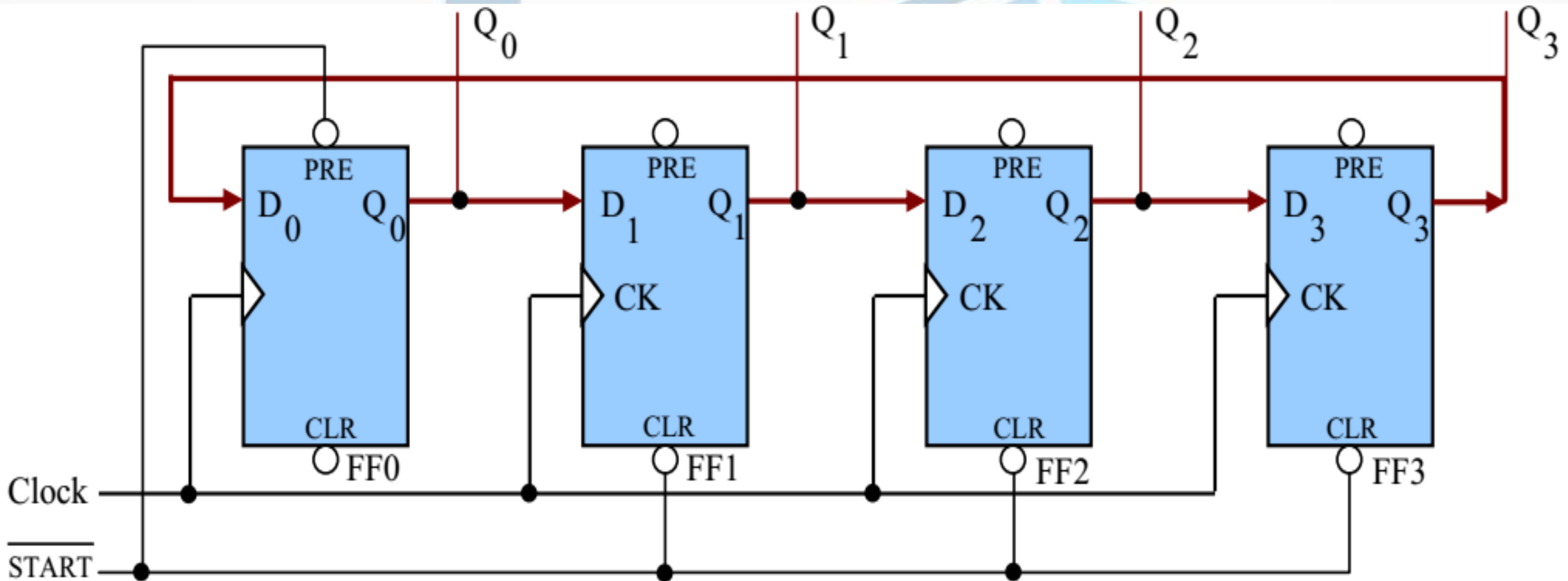
SISO Rotate Right



SISO Rotate Left

Shift Register Sequencer (Ring Counter)

مسجل الازاحة المتتابع (العداد الحلقي)



transition table Ring Counter

Clock Pulses	خرج العداد			
	Q ₀	Q ₁	Q ₂	Q ₃
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1

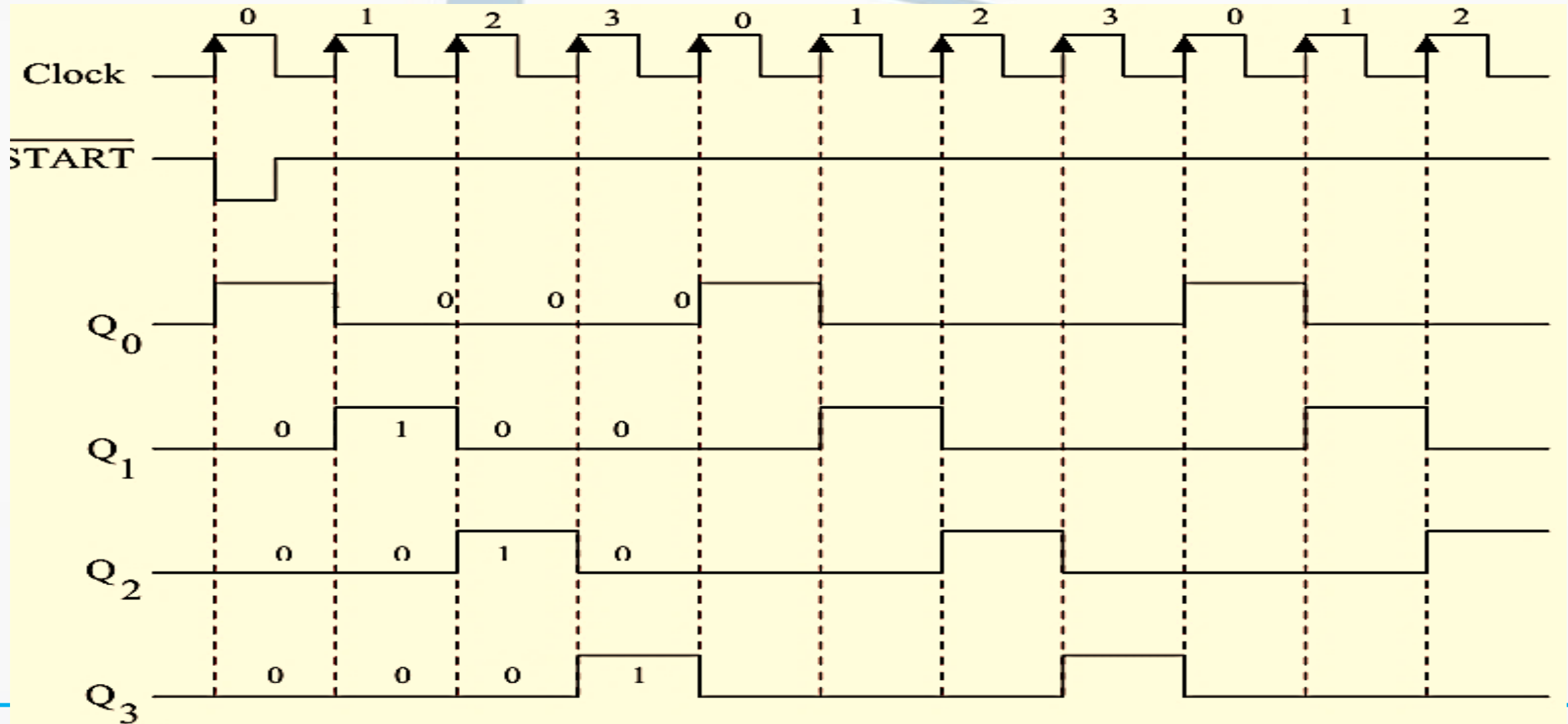
Four flip-flops will have
Four output states.

Repeat Sequence

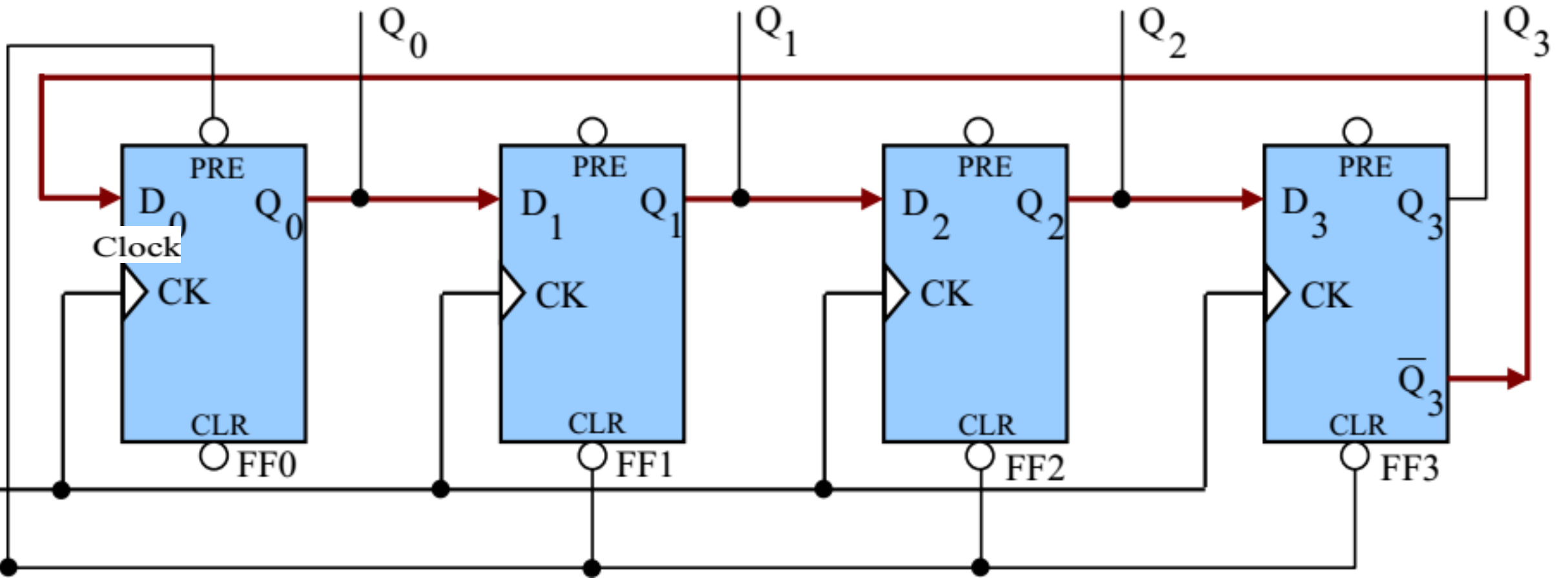
Timing Diagram Ring Counter



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Johnson Counter



transition table Johnson Counter

Clock Pulses	خرج العداد			
	Q_0	Q_1	Q_2	Q_3
0	1	0	0	0
1	1	1	0	0
2	1	1	1	0
3	1	1	1	1
4	0	1	1	1
5	0	0	1	1
6	0	0	0	1
7	0	0	0	0

\overline{Q}_3

Four flip-flops will have eight output states.

Repeat Sequence

Timing Diagram Johnson Counter

